AD 14184

ACCELERATED LIFE TESTING
OF
METALLIC RECTIFIERS

3rd QUARTERLY REPORT (January 1, March 31, 1953)

FACTORS AFFECTING LIFE CHARACTERISTICS
OF METALLIC RECTIFIERS

CONTRACT NO. DA-36-039 SC 42490

DEPARTMENT OF THE ARMY PROJECT NO. 3-99-15-022

SIGNAL CORPS PROJECT NO. 32-152 B

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1-0 Abstract

The present report describes the work done and the results achieved in the course of an investigation aimed to develop an accelerated life testing procedure for Selenium Rectifiers.

Data on standard life tests, and on tests performed under higher than normal ambient temperature or higher than normal current density are included - for a total of 88 stacks.

2-0 Purpose

2-1 This study is aimed at the gathering of quantitative data to be used as a basis for the establishment of an accelerated life testing procedure for Selenium Rectifiers.

Under Specification MIL-R-11050, SGC, such testing is now performed at rated electrical loading at normal ambient temperature and requires 3000 hours (125 days) to establish adequacy of performance.

A method of evaluation more efficient with respect to the time is highly desirable for both military and industrial users of Selenium Rectifiers.

More specifically the principal objective of this study is the establishment of a procedure which will consent, through the use of curves, tables, or formulas, to extrapolate the long life behavior of Selenium Rectifiers from the results of a comparatively short test (200 hours).

The systematic gathering of life test data on a large number of rectifiers of different makes and dimensions, under different environmental and operating conditions alone may prove to be a useful by-product of the present investigations.

3-0 Publications, lectures, reports, conferences.

3-1 Monthly Report dated February 15, 1953.

3-2 Conference - Rice Institute - Houston, Texas - February 20, 1953.
Mr. Bechtold - Mr. Gentile - Mr. McDaniel.

3-3 Monthly Report dated March 11, 1953.

4-0 Factual Data

4-1 Introduction

The useful life of Selenium Rectifiers is limited by an increase of the internal resistance in the forward direction of the current - (ageing).

The rate of ageing is dependent upon several environmental and operating factors - ambient temperature, current density in the cells, and input voltage being the most important. The fabrication technique, the cell size, the method used in grading the finished product, appear also to have a certain influence on the long life behavior of rectifiers.

To evaluate the effect of the known ageing factors and to recognize other possible influences, the program of this investigation was designed to insure the maximum possible control on each of the known ageing parameters.

Three stack sizes for each of the three recognized manufacturing techniques are being studied, conducting in effect, 9 separate and parallel investigations. Five samples of each type of stack are employed to minimize the effect of individual differences.

Because of the high acceleration of ageing desired (from 3000 to 200 h) and of the desirable simplicity of a method based on temperature and current density, these factors are investigated first.

The preliminary objectives may be succintly stated in the following manner:

(1) Determine, experimentally, the trend of ageing for stacks operating under rated conditions. This group of stacks will be referred to as the "Control Group".

(2) Determine, experimentally, the current density (as a percentage of the rated current density) capable of accelerating the process of ageing to such an extent to simulate in the shortest possible time (tentative goal 200 h), 3000 h of operation under normal conditions.

(3) Determine, experimentally, the ambient temperature capable of accelerating the process of ageing to such an extent to simulate in the shortest possible time (200 h, tentatively) 3000 h of operation under normal conditions.

4-2 **Procurement of the Stacks**

A total of 237 stacks has been procured from the three manufacturers selected in accord with the Contracting Agency. The three recognized fabrication techniques (pressed powder, evaporation, and molten dip) are represented, each in three commercial sizes. The specifications were:

Full wave bridge stacks, connected 4-1-1, rated 22-28 V_{ac} input, normal spacing, commercial coating, rated for fixed resistive load, at 35°C for the following approximate ratings:

.450 mA   2.75 A   9.5 A

were supplied.

Code	Process	Cell Size inches	Plate Spacing	No. of Stacks Procured
A_3	p.p.	5x6	5/8	20
A_2	p.p.	3x3	3/8	20
A_1	p.p.	1-1/4x1-1/4	1/8	40
B_3	ev.	5x6	1/2	20
B_2	ev.	3x3	3/16	20
B_1	ev.	1-1/2x1-1/2	3/16	37
C_3	m.d.	4-1/4x6	5/16	20
C_2	m.d.	3-3/8 Dia.	5/16	20
C_1	m.d.	1-3/8 Dia.	3/16	40

4-3 **Administration of the Stacks**

A progressive serial number is assigned to each stack upon reception. The initial characteristics [V_{output}, I_{Rev}, $V_{sch\text{-}circuit}$], the disposition of the stack, and the final characteristics are recorded.

Table I shows the initial and final characteristics of all the stacks used up to March 31, 1953.

4-4 <u>Description of Facilities</u>

4-4-1 Room temperature tests (30° Ambient)

The complete description of the facilities employed to perform the tests at ambient temperature will be found in the I Quarterly Report. No significant changes were made to the original apparatus.

4-4-2 High Ambient Temperature Tests

The apparatus employed in performing the high ambient temperature tests has been described in the I Quarterly Report.

A thermostatically controlled switch has been added; should the ambient temperature rise above a prefixed limit, all the stacks will be automatically deenergized.

4-5 Recording and Interpretation of Data

Input and output voltage, Plate and Room temperature, Input and Output current are read and recorded regularly.

Curves of V_{output} vs. time are drawn for every stack tested.

The data are recorded as shown in Table IV: Fig. (1) shows a sample curve of V_{output} vs. time.

Only average and significant data are included in the present report. However, the individual data and the relative curves are kept in the Project's file.

They will be made available upon request approved by the Contracting Agency.

The make of the stacks is indicated by Code Letter (A - B - C): Appendix <u>A</u>, separately enclosed to the report and marked <u>Confidential</u>, supplies the Code's key.

4-6 <u>Control Group</u>

The control group consists of 45 stacks (5 units for each of the 9 types) operating at room temperature (30°C), at rated load and rated input voltage.

The output voltage, corrected to 26 volts input by linear interpolation, is plotted vs. time in Figs. 2-3-4-5-6-7-8-9-10-11-12. A_1, A_2, C_1, C_2 stacks exhibit marked similarity of behavior among the 5 units; in the other stacks more than one trend is evident.

A study was made to investigate possible relationship between the initial characteristics (I reverse and $V_{sch.circuit}$) and the slope of the curves V_{output} vs. time: No significant correlation is apparent. For example - comparing stacks 1-2 with 3-4-5

	1	2	3	4	5
V_{out} (initial)	21.2	21.09	20.65	20.60	20.72
I_{Rev} (" ")	37.6	22	13.3	13.1	9.3
$V_{sch.c.}$ (" ")	3.66	2.92	2.95	2.93	2.96
Plate temperature raise (initial)	17°	14°	17°	21°	19°
V_{out} (after 100 days)	20.53	20.40	19.42	19.63	19.43
$I_{Rev.}$ (" ")	66.	30.5	21.8	20.2	12.4
$V_{schc.}$ (" ")	2.88	2.96	3.34	3.23	3.33
Plate temperature raise (after 100 days)	18°	15°	23°	20°	24°

Higher reverse current and higher initial voltage seem to correlate with lower rate of ageing; while no apparent connection exists between short circuit voltage and the slope of the V_{output} curve. Comparing stacks 6-7-8-9-10 :

	6	7	8	9	10
V_{out} (initial)	21.3	21.53	21.60	21.53	21.52
$I_{Rev.}$ (" ")	29.9	8.5	27.3	20.7	7.6
$V_{schc.}$ (" ")	2.25	2.29	2.10	2.08	2.21
Plate temperature raise (initial)	10°	14°	14°	14°	14°

	6	7	8	9	10
V_{out} (after 100 days)	21.03	21.16	21.23	21.15	21.28
$I_{Rev.}$ (" ")	20.5	10.0	29.7	24.6	11.3
$V_{schc.}$ (" ")	2.09	2.12	2.02	2.07	2.05
Plate temperature rise (after 100 days)	10°	9°	11°	12°	10°

Stacks 7 and 10 do not show any appreciable difference in ageing with respect to 6-8-9 regardless of the comparatively lower $I_{Rev.}$ and higher V_{output}. The investigation was extended to other stacks with the same negative results.

The discontinuity noticeable on some of the curves (Figs. 2-3-5-8-9-11) seems to point to a common external factor: on or about February 20, 1953, most of the stacks exhibited a sudden increase in output voltage. The secondary voltmeter chart did not show any apparent reason for the phenomenon, nor does the project's log indicate any abnormal event on or about that time.

Plate temperature and plate temperature rise vs. time were plotted for stacks 11-12-13 and 22-23-24-25-26. No significant trend was detectable and they are not included in the present report.

4-7-0 <u>Tests at room temperature and higher than rated current density</u>.

4-7-1 Three samples of each type, C_3 excepted, were tested at ambient temperature rated input voltage, and 1.73 times rated current. Figs. 13-14-15-16-17-18-19-20 show graphically, V_{output} vs. time.

In general some qualitative correlation exists between those stacks and the corresponding control group.

For instance, the stacks A_3, which exhibit marked differences in the control group, also show different rates of ageing when operated at $\sqrt{3}$ times rated current.

Even considering that the data from only 3 samples could be relied upon only to a certain extent, the average rate of ageing was considered too low to warrant further investigation, with the exception of stacks A_3. The test was suspended after 75 days to investigate the effect of higher current density.

4-7-2 Three samples of each small size (A_1-B_1-C_1) were tested at ambient temperature, rated input voltage, and 3 times rated current.

Stacks 101-102-103-122-124-128-34-35-36, Figs. 22-23 -

The Stacks A_1 aged rapidly and erratically: that is each one exhibited a different and variable rate of ageing. Not enough points were collected to warrant the drawing of a curve. The 3 stacks B_1 showed definite uniformity of behavior and no appreciable drop in output voltage after 53 days. (Fig. 22): the test continues. The 3 stacks C_1 aged considerably and regularly but each one in a different way. (Fig. 23).

Type A_1 seems to be affected to a point of rapid destruction. Type B_1 does not show appreciable effect, and type C_1 exhibits a definite trend.

Three more A_1 (63-64-74) were tested at $\sqrt{5}$ times rated current (Fig. 21): they aged consistently but at an unsatisfactory slow rate.

4-8-1 Test at rated Input voltage, rated current, and high temperature. (90° Ambient)

Eighteen stacks (3 A_1, 3 A_2, 3 A_3, 3 B_3, 3 C_1, 3 C_2) were simultaneously tested at 90°C ambient temperature, at rated current, and rated input voltage. Curves 24-25-26-27-28-29 show, graphically, output voltage vs. time.

Only the A_1 stacks exhibited enough similarity of behavior to warrant the averaging of the data among the 3 samples.

All the others showed different rates of ageing for each unit; no generalization was possible. The test was interrupted after 26 days by a sudden rise in the ambient temperature (above 150°C) with consequent destruction of all the stacks. Each stack was individually protected on the input with fuses and the cooling apparatus was found in good operating condition. The only explanation for the sudden rise seems to be a rapid and simultaneous increase of the heat losses of the stacks, due to ageing.

A circuit breaker, thermostatically controlled, was added on the power input line to disconnect all the stacks should the temperature rise above a prefixed limit.

4-8-2 75°C Ambient Test

Six stacks (3 A_1 and 3 B_1) were tested at rated input voltage, rated output current, and 75°C ambient temperature.

The stacks A_1 (Fig. 30) exhibited considerable individual differences: stacks B_1 (Fig. 31) showed similarity of behavior. The test continues.

4-9-0 Investigation of stacks, operating inside of a small thermally insulated enclosure.

4-9-1 This test was originally conceived to study the effects of high plate temperature on forward resistance.

In the tests at high plate temperature, the effect of ageing on the output voltage is partially offset by the decrease in resistivity due to the rise in temperature.

When a stack is operating under load inside of a small Dewer Flask, the plate temperature rises rapidly because of the poor heat transfer coefficient of the enclosure.

Fig. 23 shows V_{output} vs. plate temperature for a C_1 stack operating at rated V_{input} and I_{output}.

However, as shown in Fig. 33, the stack exhibits considerable ageing in a comparatively short time.

It did appear then, that a procedure based on this principle could be devised to accelerate the ageing of the stacks.

The simplicity and short duration of a test of this type are such that a further study seems to be justifiable.

5-0 Conclusions

The control group (5 units for each type) exhibited a rather uniform ageing among stacks of the same type with the exception of A_3 and C_1, where more than one trend is evident.

However, at the end of the period covered by the present report, after about 160 days of operation, individual differences are becoming evident.

It appears that, although the ageing is rather uniform in the early period of life, later the individual differencesamong the stacks become more and more pronounced.

This observation is confirmed by the results of the accelerated test, especially when the rate of ageing is considerably increased (Fig. 23).

The tests at 1.73 times rated current (4-7-1) and 75°C ambient (4-8-2) showed very little ageing.

In general the results of all the tests indicate more individual deviations than expected. All the tests which have shown promising results will have to be confirmed on a much larger number of stacks.

6-0 Program for the next interval

The life test of the control units will be continued.

The test at three times rated current will be performed on all the other types of stacks (A_2-A_3-B_2-B_3-C_2-C_3) (three of each). Another set of A_1 will be tested at three times rated current to confirm rapid ageing of the first units tested.

Stacks B_1 and C_1 will be tested at four times and 3.5 times rated current, respectively.

The Dewar Flask test will be performed on all the small stacks: in case of promising results, a testing apparatus will be built to consent the test of more than one stack at the time.

7-0 Identification of Key Technical Personnel

7-1 Gentile, Ralph G.

Dr. El. Eng. - University of Rome (Italy) - 1938
Lieut. Eng. Italian Air Forces - Research and Dev. - 1939-1942
Research Engineer - F.A.T.M.E. - Rome (Italy) 1942-1943
Research Engineer - U.S. Government - Newport (R.I.) - 1943-1944
Chief Engineer - T.R.M. El. Co. - Middletown (Conn). - 1944-1949
Assistant Professor Electrical Engineering - The Rice Institute - 1949 -

Hours of work performed during present quarter 300

7-2 McDaniel, George

B.A. - The Rice Institute, Houston, Texas - 1952
Summer Employment -
Sun Oil Co. - Electric and Communication Department
1948 - 1949 - 1950 - 1951
Graduate Student working toward a Master of Science Degree in Electrical Engineering at the Rice Institute

Hours of work performed during present quarter 260

7-3 Smythe, Robert C.

B.A. - The Rice Institute, Houston, Texas - 1952
Summer Employment -
Trans-Texas Airways, Communication Department
Working toward Bachelor of Science Degree in Electrical Engineering

Hours of work performed during present quarter 200

TABLE I

CHARACTERISTIC OF STACKS

Stack No.	Initial Characteristics V out	I rev mA	V.sc	Final Characteristics V out	I rev mA	V.sc	Test	Type
1	21.20	37.6	2.66				Control	A3
2	21.08	22.1	2.92				" "	A3
3	20.65	13.3	2.85				" "	A3
4	20.60	13.1	2.83				" "	A3
5	20.72	9.3	2.96				" "	A3
6	21.50	29.9	2.25				" "	A2
7	21.53	8.5	2.28				" "	A2
8	21.60	22.2	2.10				" "	A2
9	21.53	20.7	2.08				" "	A2
10	21.52	7.6	2.21				" "	A2
11	20.86	3.54	2.55				" "	A1
12	20.59	2.80	2.51				" "	A1
13	20.82	3.82	2.60				" "	A1
14	20.63	2.66	2.38				" "	A1
15	20.32	2.89	2.68	15.60	5	6.55	" "	A1
16	21.25	6.44	2.30				" "	B1
17	21.26	6.49	2.63				" "	B1
18	21.48	29.9	2.45				" "	B2
19	21.43	20.8	2.28				" "	B2
20	21.24	181.	2.86				" "	B3
21	20.90	99.	3.37				" "	B3
22	20.89	28.9	2.56				" "	C1
23	20.74	21.9	2.77				" "	C1
24	20.89	33.3	2.73				" "	C1
25	20.57	26.0	2.92				" "	C1
26	20.79	33.2	2.77				" "	C1
27	21.46	148.	2.45				" "	C2
28	21.27	130.	2.68				" "	C2
29	21.30	130.	2.62				" "	C2
30	21.01	118.	2.95				" "	C2
31	21.30	148.	2.76				" "	C2
32	-	-	-				--	--
33	20.42	19.2	2.70				3I	C1
34	20.18	12.6	3.11	19.40	17.5	3.68	3	C1
35	20.28	26.8	3.02	19.00	26.5	4.26	3	C1
36	20.02	28.2	3.15	19.60	38.0	3.28	3	C1
37	-	-	-				-	--
38	20.11	16.8	3.25	19.30	27.0	3.92	√3	C1
40	21.50	33.3	2.12	20.20	14.0	2.96	√3	A2
50	21.50	29.8	2.00				Control	B1
51	21.45	58.0	2.03				" "	B1
52	20.60	20.9	2.80	19.60	9.0	3.62	√3	B1
53	21.60	70.3	2.00				Control	B1
54	20.95	21.0	2.60	20.00	15.0	3.20	√3	B1
55	20.65	5.73	2.79	20.00	16.0	3.24	√3	B1
57	20.59	8.7	2.85	19.00	20	4.12	75°	B1
61	21.50	21.5	1.96		Destroyed			A1
62	20.00	27.5	2.71		Shorted		75°	A1
63	21.60	4.0	1.95				√5	A1
64	21.30	10.0	2.12				√5	A1
65	21.60	8.7	1.20		Destroyed		90°	A1

TABLE I - CHARACTERISTICS OF STACKS (Continued)

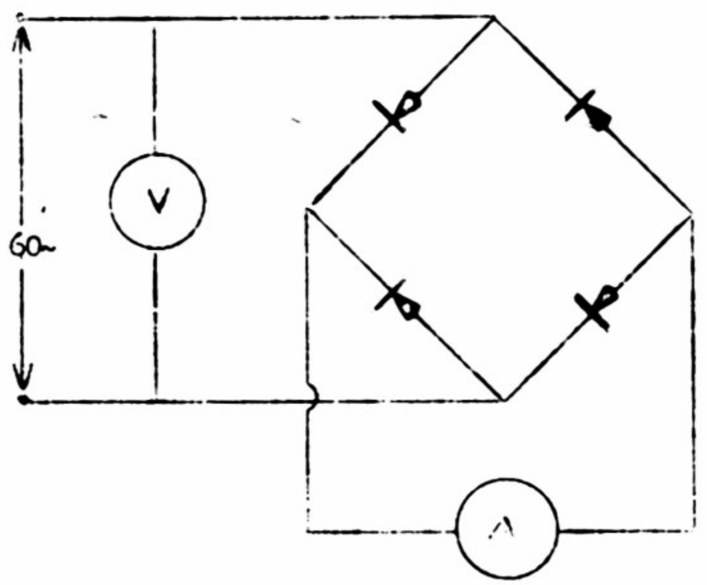
Stack No.	Initial V out	Characteristics I rev mA	V.sc.	Final V out	Characteristics I rev mA	V.sc.	Test	Type
66	21.50	7.4	2.00		Destroyed		90°	A1
67	20.24	29.5	3.03	18.50	26.0	4.80	Thermos	
68	19.78	19.8	3.36				Thermos	C1
69	20.20	32.0	3.10				" "	C1
70	20.60	25.0	2.97		Destroyed		90°	C1
71	20.95	30.0	2.37		" "		90°	C1
72	20.40	39.6	3.20		" "		90°	C1
73	21.31	6.55	2.08	20.45	4.0	2.68	√3	A1
74	21.32	4.6	1.80				√5	A1
75	--	--	--				75°	A1
76	--	--	--				√3	A1
83	21.04	63.0	2.26	19.60	50.0	3.32	√3	A3
84	21.40	90.9	2.79	19.40	460.	3.44	√3	A3
85	--	--	--				√3	C1
86	21.30	133.	2.62		Destroyed		90°	C2
87	21.40	108.	2.38		" "		90°	C2
88	20.60	120.	3.12		" "		90°	C2
89	20.50	102.	--	19.60	193.	3.42	√3	C2
90	20.59	93.0	--	19.70	208.	3.30	√3	C2
91	20.80	18.5	2.84		Destroyed		90°	A3
92	21.00	16.5	2.76		" "		90°	A3
93	21.00	15.0	2.82		" "		90°	A3
94	21.00	15.0	2.94	17.58	18.4	5.21	√3	A3
95	21.00	21.1	2.99	16.50	10.0	6.00	√3	A3
96	21.20	12.9	2.00	18.30	6.0	4.80	√3	A2
97	21.16	10.2	-	19.80	9.0	3.26	√3	A2
98	21.60	22.0	2.00		Destroyed		90°	A2
99	21.50	21.5	2.08		" "		90°	A2
100	21.60	23.0	2.03		" "		90°	A2
101	20.90	2.81	2.37	9.00	1494.	5.00	3I	A1
102	20.67	1.33	2.35	17.90	1.0	4.98	3I	A1
103	20.80	3.10	2.36	17.80	1.0	4.81	3I	A1
104	21.00	5.90	2.25	17.40	4.0	5.07	√3	A1
105	20.50	1.00	2.53		Shorted		75°	A1
106	20.95	22.8	3.30		Destroyed		90°	B3
107	21.40	96.	2.80				Control	B3
108	21.00	29.9	3.25		Destroyed		90°	B3
109	21.40	20.3	2.76				Control	B3
110	21.50	123.	2.66				" "	B3
111	21.00	101.	3.20		Destroyed		90°	B3
112	21.00	109.	3.19	19.40	140.	3.86	√3	B3
113	20.95	77.	3.29	19.15	118.	3.98	√3	B3
114	21.37	139.	2.69	19.40	214.	3.60	√3	B3
115	20.78	29.5	2.86				Control	B2
116	20.95	23.1	2.71	20.00	26.0	3.40	√3	B2
117	20.85	38.3	2.71	19.70	40.0	3.64	√3	B2
118	20.78	30.0	2.79				Control	B2
119	20.85	29.5	2.74	20.15	40.0	3.38	√3	B2
120	21.00	17.4	2.66				Control	B2
121	20.48	8.0	3.02				Thermos	B1
122	21.45	17.1	2.00	21.00	30	2.20	3	B1

TABLE I - CHARACTERISTICS OF STACKS (Continued)

Stack	Initial	Characteristics		Final	Characteristics		Test	Type
No.	V out	I rev mA	V.sc.	V out	I rev mA	V.sc		
124	21.42	22.2	2.00	21.00	29	2.24	3	B1
128	21.40	22.7	2.00	20.80	49	2.50	3	B1
130	20.64	7.4	2.80	19.40	44	3.86	75°	B1
131	21.40	8.9	2.06	18.90	114	3.68	Thermos	B1
134	20.66	6.5	2.80				75°	B1
135	20.72	8.7	2.70				Thermos	B1
137	21.15	399.	3.21				Control	C3
139	20.62	469.	3.21				" "	C3
140	20.75	300.	3.07				" "	C3
149	20.61	312.	3.36				" "	C3
154	20.60	570.	3.21				" "	C3
159	20.30	104.	2.86				3I	C2
161	20.40	252.	2.84	16.80	343	6.80	3I	C2
165	20.40	80.	2.72	19.60	184	3.56	3I	C2
188	20.50	4.0	2.56				Thermos	A1
189	20.40	4.0	2.52	16.98	520.	3.45	" "	A1
190	20.55	5.0	2.58	15.60	--	--	" "	A1
191	20.60	6.0	2.24				3I	A1
192	20.48	5.0	2.40	16.9	14	5.05	3I	A1
193	20.52	5.0	2.40				3I	A1
194	20.40	4.0	2.42	19.35	234.	3.40	Thermos	A1
208	21.10	14.0	1.97	20.80	4.0	2.40	" "	D1

TABLE II

TEST CIRCUIT FOR FORWARD CONDUCTANCE TEST

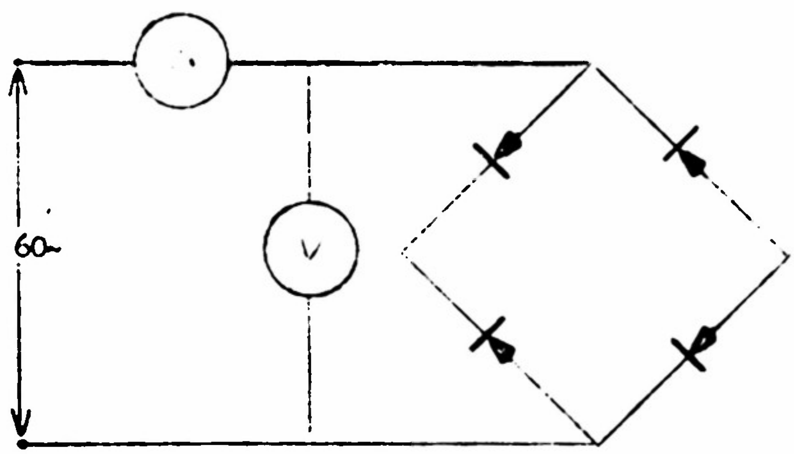


NOTES:

(V) Voltmeter, C5A. Weston Model 155, 0-5 volts.

(A) Ammeter, B4B, Weston Model 45, 0-1.5, 0-3, & 0-15 amperes, with External Shunts

TEST CIRCUIT FOR REVERSE CURRENT TEST



NOTES:

(V) Voltmeter, S21. Weston Model 341, 0-30 & 0-60 volts

(A) Milliammeter, L4A. Weston, Model 433, 0-50 & 0-100 mA.

or

Milliammeter, L5A, Weston, Model 433, 0-250 & 0-500 mA.

TABLE III

LIST OF METERS USED

VOLTMETERS:

S21	WESTON, Model 341, 0-30 & 0-60 Volts.
A9C	WESTON, Model 45, 0-30, 0-150 & 0-300 Volts.
C5A	WESTON, Model 155, 0-5, 0-24, & 0-120 Volts.
S22	WESTON, Model 341, 0-7.5 & 0-15 Volts.

AMMETERS:

L1E	WESTON, Model 622, 0-2, 5, 10, 20, 50, 100, 200, 500 mA.
D8C	WESTON, Model 433, 0-10 & 0-20 Amps.
B4B	WESTON, Model 45, 0-1.5, 0-3 & 0-15 Amps.
L4A	WESTON, Model 433, 0-50 & 0-100 mA.
L5A	WESTON, Model 433, 0-250 & 0-500 mA.
B11B	GENERAL ELECTRIC, Model BDP9ACW1, 0-2, 0-10 & 0-50 Amps.
B12B	GENERAL ELECTRIC, Model 3DP9ACW1, 0-2, 0-10 & 0-50 Amps.

POTENTIOMETERS:

K2E	LEEDS & NORTHRUP Thermocouple Potentiometer, 0-200°C.

TABLE V

CODE	CELL SIZE (In. x In.)	RATED CURRENT (AMPS)	$\sqrt{3}\ I_r$ (AMPS)	$\sqrt{5}\ I_r$ (AMPS)	$3\ I_r$ (AMPS)
A_1	1-1/4 x 1-1/4	0.45	.78	1.0	1.35
A_2	3 x 3	2.75	4.75	---	---
A_3	5 x 6	9.5	16.5	---	---
B_1	1-1/2 x 1-1/2	0.75	1.3	---	2.25
B_2	3 x 3	2.75	4.75	---	---
B_3	5 x 6	9.5	16.5	---	---
C_1	1-3/8 dia.	0.45	.78	---	1.35
C_2	3-3/8 dia.	2.75	4.75	---	---
C_3	4-1/4 x 6	9.5	--	---	---

STACK NO. 21 POSITION 2

MFG.NO. - - - CODE B3

RATED V 26.00 RATED I 9.5

POSITION	DATE	TIME	TIME ELAPSED	V INPUT	V OUTPUT	I OUTPUT	I INPUT	ADJUSTED I OUTPUT	ADJUSTED V OUTPUT	TABLE IV. PLATE C°	ROOM C°	I. REV. mA	V.SCH.C	V INPUT CORRECTED TO 26 V.			OPERATOR
METERS				S21	A9C	B11B	D8C	B11B	A9C	K2E	K2E	L4A L5A S21	L5F				
	1-3	1300	82	25.55	20.25	-	-	-	-	47.5	29.7	-	-	20.59			A.A.
	1-3	1300	82	-	20.20	9.73	-	-	-	-	-	-	-	-			A.A.
	1-5	1600	84	-	-	-	10.36	-	-			106	3.29	-			R.S.
	1-6	1300	85	25.15	19.90	-	-	-	-	48.0	32.7	-	-	20.57			A.A.
	1-6	1300	85	-	20.20	9.70	-	-	-	-	-	-	-	-			A.A.
	1-10	1500	89	25.90	20.70	-	-	-	-	48.0	30.7	-	-	20.77			A.A.
	1-10	1700	89	-	-	-	-	-	-	-	-	-	-	-			A.A.
	1-12	1330	91	-	19.90	9.30	-	-	-	-	-	-	-	-			A.A.
	1-13	1300	92	25.40	20.10	-	-	-	-	48.0	32.7	-	-	20.58			A.A.
	1-17	0900	96	25.25	19.95	-	-	-	-	45.0	28.5	-	-	20.55			A.A.
	1-17	1330	96	-	19.95	9.32	-	-	-	-	-	-	-	-			A.A.
	1-20	1330	99	25.10	19.90	-	-	-	-	46.5	32.2	-	-	20.62			A.A.
	1-20	1600	99	-	19.93	9.32	-	-	-	-	-	-	-	-			A.A.
	1-24	1230	103	25.14	19.91					49.5	30.0	-	-	20.60			A.A.
	1-24	1500	103	-	19.80	9.27	-	-	-	-	-	-	-	-			A.A.
	1-31	1400	110	24.92	19.80	-	-	-	-	51.5	33.0	-	-	20.60			A.A.
	2-3	1300	113	24.91	19.70	-	-	-	-	49.5	31.0	-	-	20.60			A.A.
	2-3	1300	113	-	19.70	9.15	-	-	-	-	-	-	-	-			A.A.
	2-7	1345	117	25.45	20.10	-	-	-	-	-	-	-	-	20.50			A.A.
	2-13	1430	123	25.10	19.80	-	-	-	-	50.0	30.5	-	-	20.50			H.
	2-16	1300	126	25.35	20.10	-	-	-	-	49.0	32.5	-	-	20.60			P.
	2-16	1700	126	-	19.60	9.20	-	-	-	-	-	-	-	-			P.
	2-17	1700	127	-	-	-	10.08	-	-	-	-	99	-	-			H.
	2-20	1400	130	25.50	20.60	-	-	-	-	48.0	29.5	-	-	21.00			H.
	2-20	1700	130	-	20.00	9.20	-	-	-	-	-	-	-	-			H.
	2-23	1315	133	25.10	20.40	-	-	-	-	46.0	27.0	-	-	21.14			P.
	2-23	1315			20.00	9.20	-	9.50	19.9	-	-	-	-				P.
	2-24	1400	134	-	-	-	-	-	-	-	-	-	3.28	-			H.
	2-27	1300	137	25.15	19.85	-	-	-	-	50.0	31.5	-	-	20.52			H.

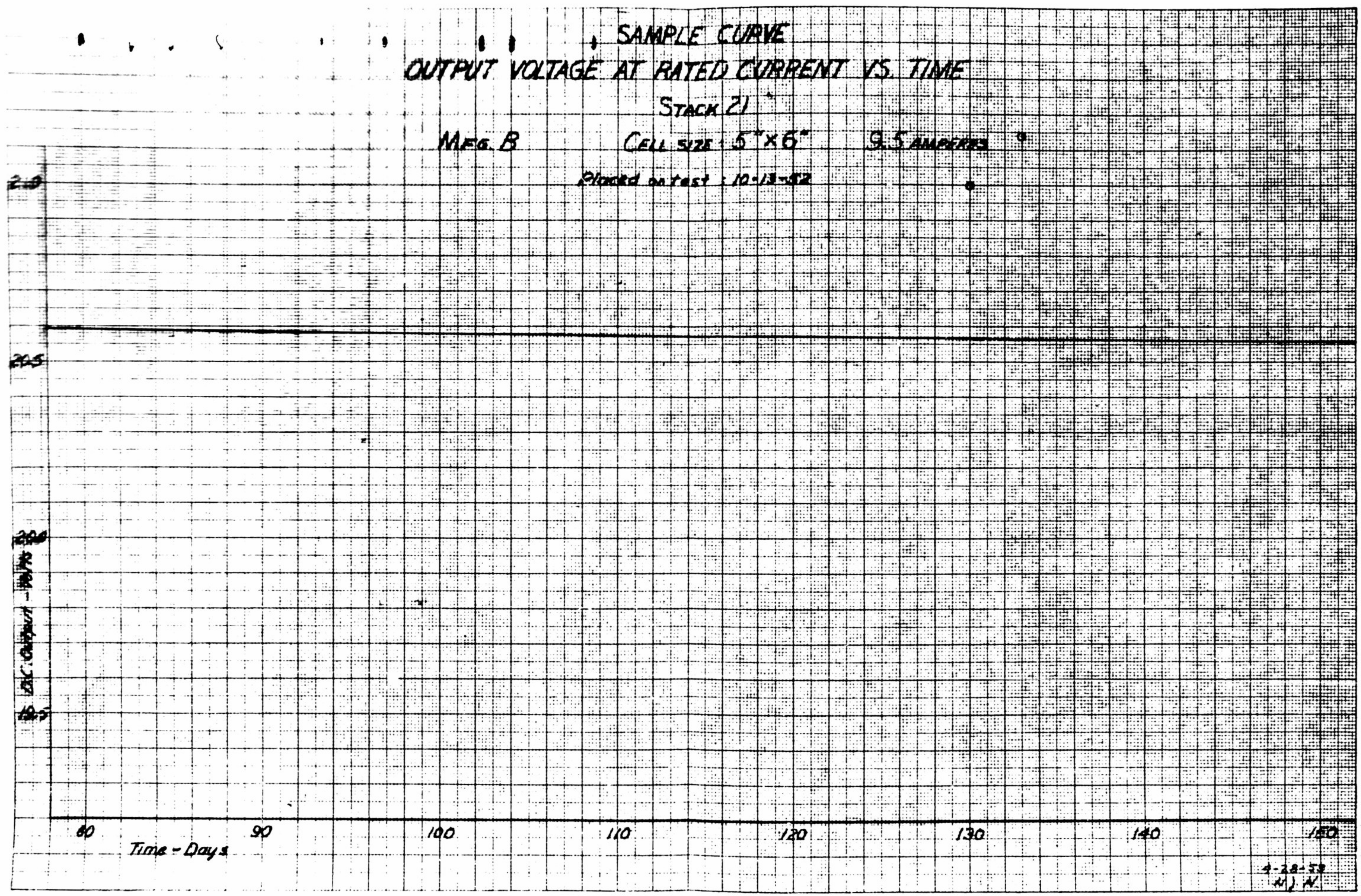
TABLE IV (continued)

STACK NO. 21 POSITION 2

MFG.NO. ---- CODE B3

RATED V 26.00 RATED I 9.5

METERS	POSITION	DATE	TIME	TIME ELAPSED	V INPUT	V OUTPUT	I OUTPUT	I INPUT	ADJUSTED I OUTPUT	ADJUSTED V OUTPUT	PLATE C°	ROOM C°	I. REV. mA	V.SCH.C	V INPUT CORRECTED TO 26 V.			OPERATOR	NOTES
		2-27	1500	137		19.70	9.45											H.	
		3-2	1300	140	25.10	19.90					49.7	32.0			20.60			P.	
		3-6	1330	144	25.25	19.85					48.7	31.0			20.45			H.	
		3-6	1500	144		19.95	9.55											H.	Tightened loose connection to bus.)
		3-9	1300	147	25.55	20.20					49.0	31.0			20.58			P.	3-7-53 R.S.)
		3-9	1300	147		20.10	9.50											P.	
		3-10	1430	148										3.08				R.S.	
		3-13	1300	151	24.90	19.85					50.5	35.0			20.73			P.	
		3-16	1315	154	25.25	20.00					49.0	34.0			20.60			P.	
		3-16	1315	154		20.40	9.5											P.	
		3-17	1445	155				10.85					89					H.	
		3-20	1630	158	26.00	20.60					51.0	31.0			20.60			H.	
		3-20	1500	158		20.20	9.70											H.	
		3-23	1300	161	25.60	20.31					52.0	32.0			20.62			P.	
		3-23	1300	161		20.20	9.60											P.	
		3-24	1530	162										3.30				H.	
		3-27	1400	165	24.10	19.10					52.0	35.0			20.60			H.	
		3-27	1530	165		18.85	8.75											H.	
		3-30	1245	168	24.62	19.42					51.0	33.0			20.49			P.	
		3-31	1530	169				10.45					101					H.	



SAMPLE CURVE
OUTPUT VOLTAGE AT RATED CURRENT VS. TIME
STACK 21
MFG. B
CELL SIZE 5" x 6"
9.5 AMPERES
Placed on test: 10-13-52
21.0
20.5
20.0
19.5
D.C. Output - Volts
80
90
100
110
120
130
140
150
Time - Days
4-28-53
W. J. W.

Fig. 1

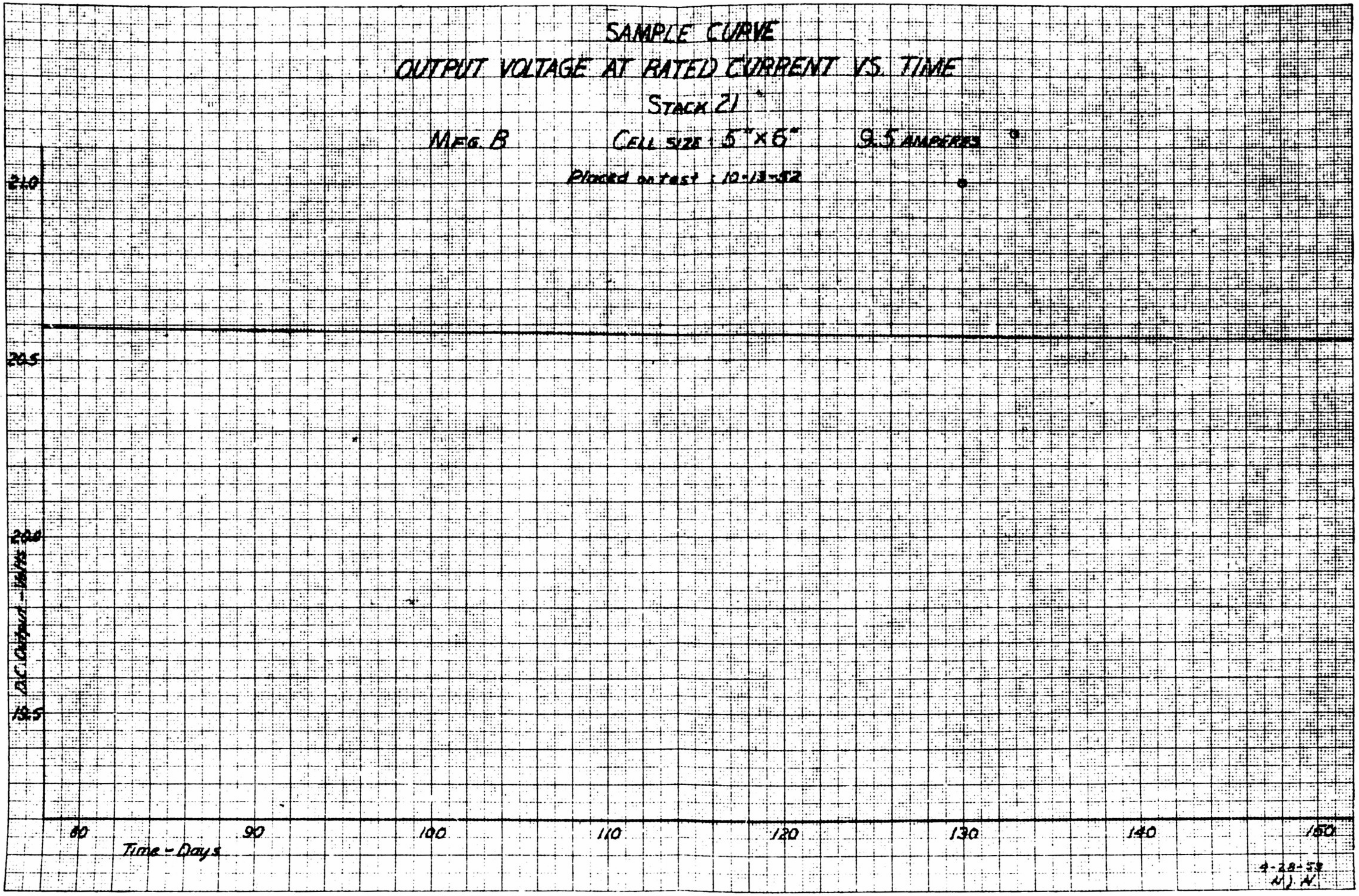

SAMPLE CURVE
OUTPUT VOLTAGE AT RATED CURRENT VS. TIME
STACK 21
MFG. B
CELL SIZE 5"×6"
9.5 AMPERES
Placed on test : 10-13-52
21.0
20.5
20.0
19.5
D.C. Output - Volts
80
90
100
110
120
130
140
150
Time - Days
4-28-53
N. J. N.

Fig. 1

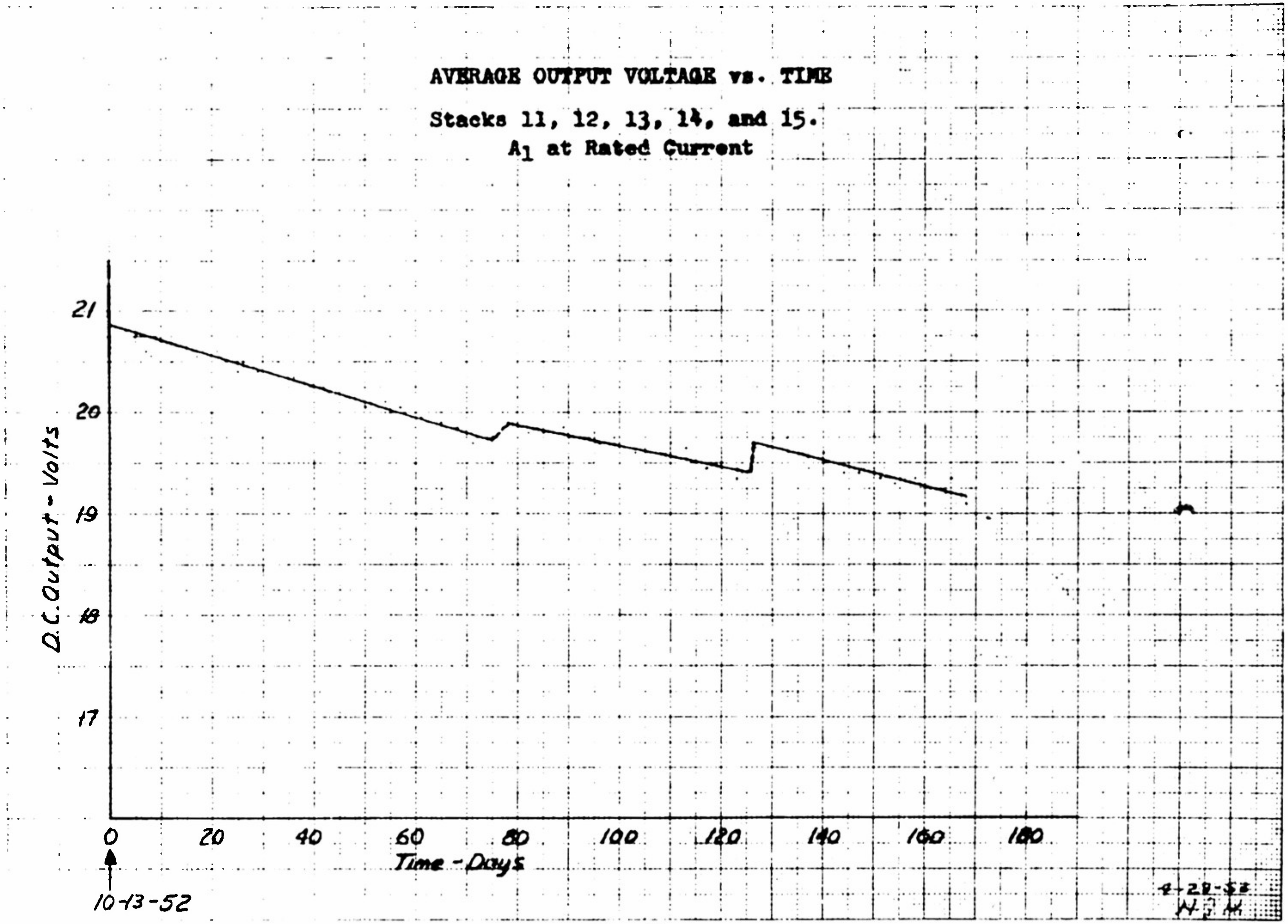

AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 11, 12, 13, 14, and 15.
A1 at Rated Current
D.C. Output - Volts
21
20
19
18
17
0
20
40
60
80
100
120
140
160
180
Time - Days
10-13-52

Fig. 2

AVERAGE OUTPUT VOLTAGE vs. TIME

Stacks 6, 7, 8, 9, and 10.
A_2 at Rated Current

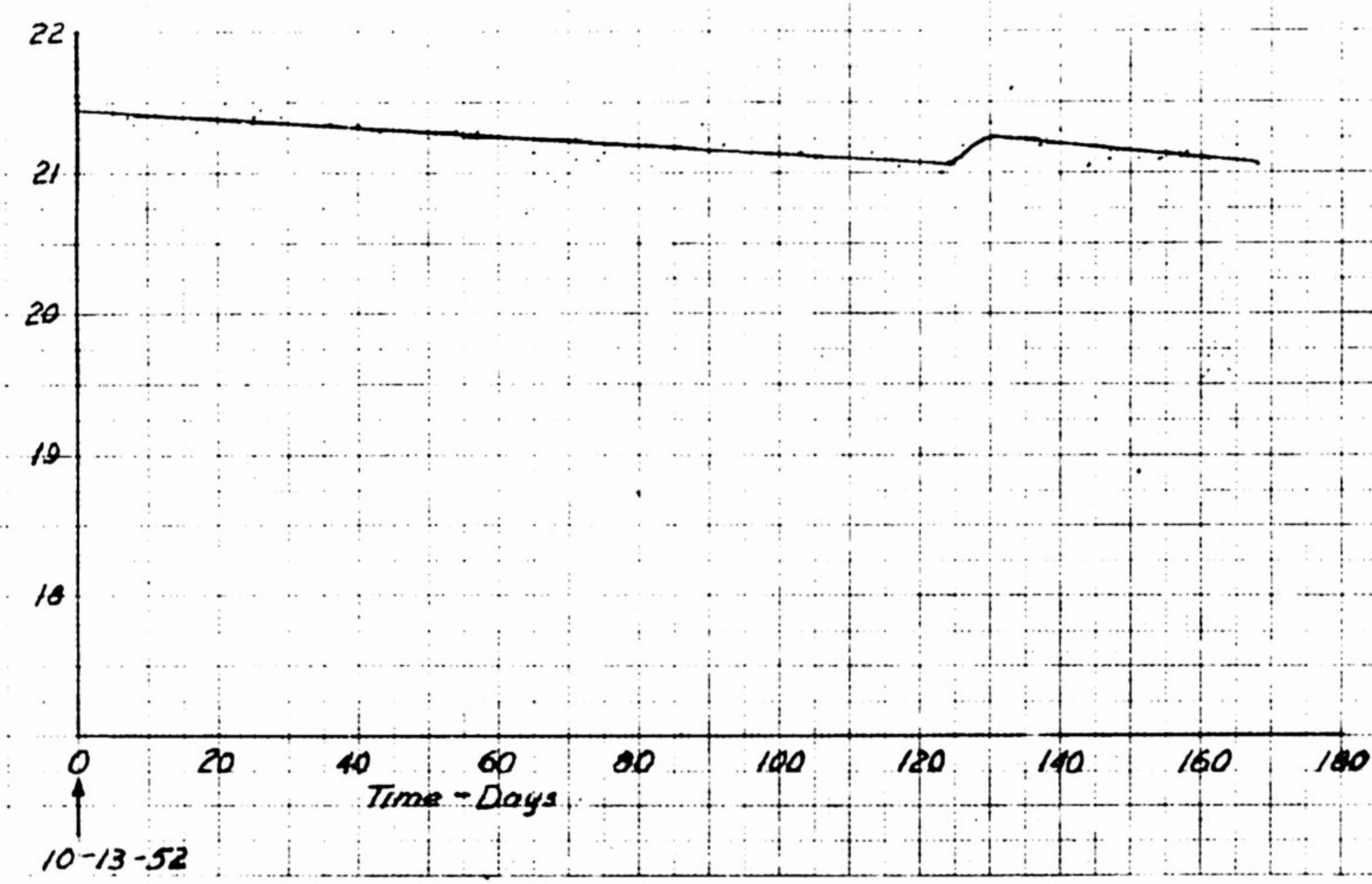
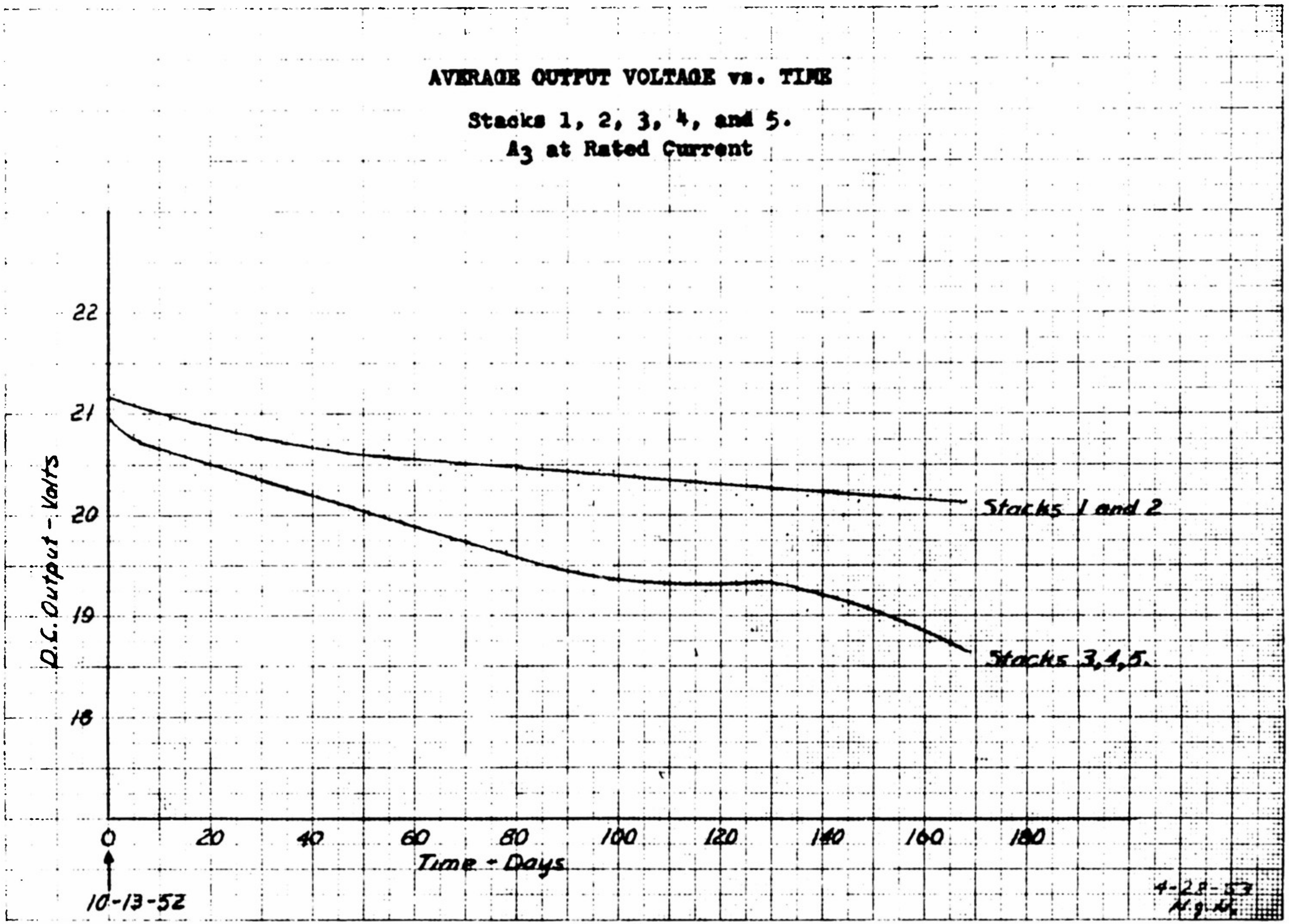


Fig. 3



AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 1, 2, 3, 4, and 5.
A_3 at Rated Current
22
21
20
19
18
D.C. Output - Volts
0
20
40
60
80
100
120
140
160
180
Time - Days
10-13-52
Stacks 1 and 2
Stacks 3,4,5.

Fig. 4

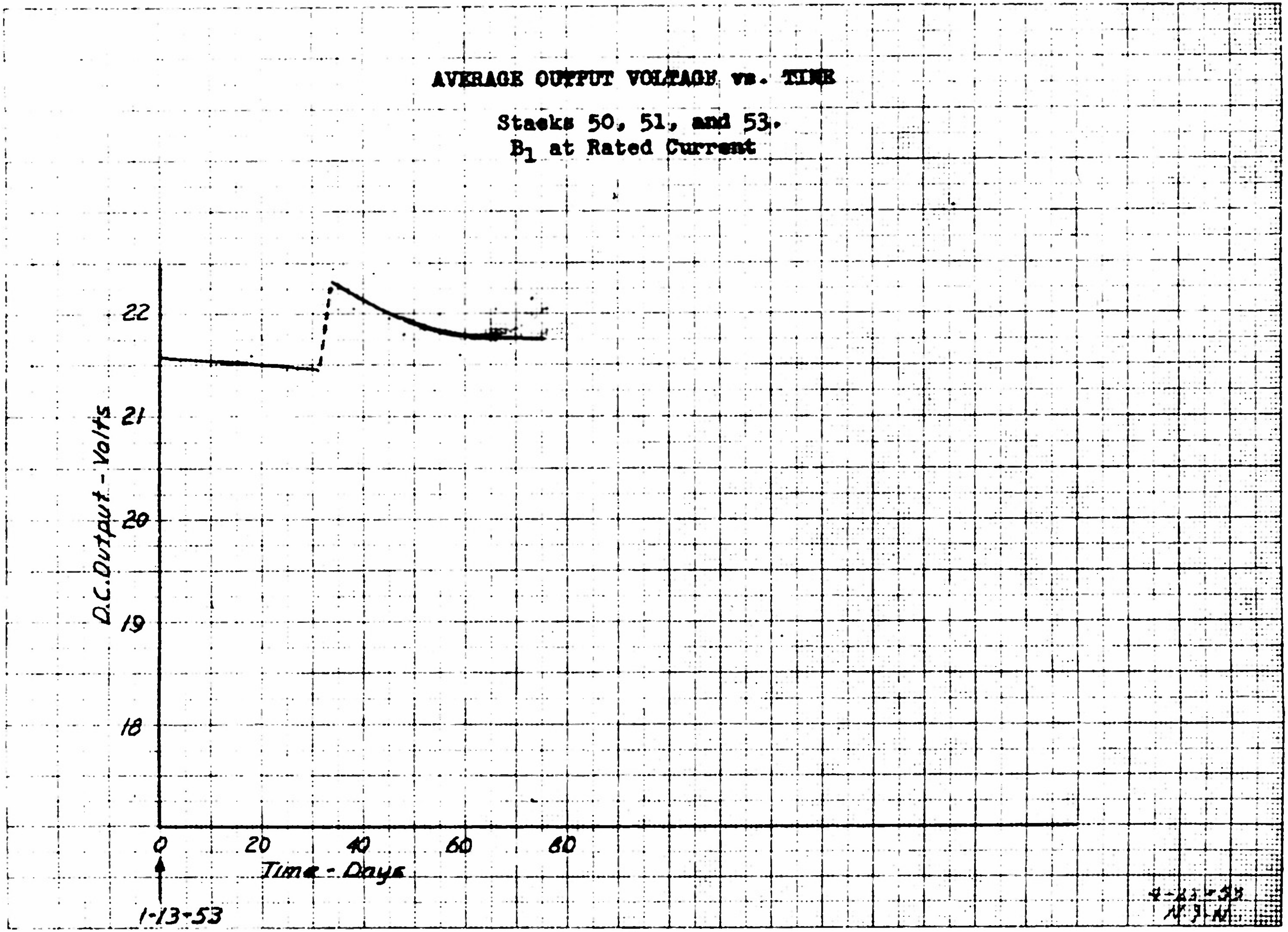
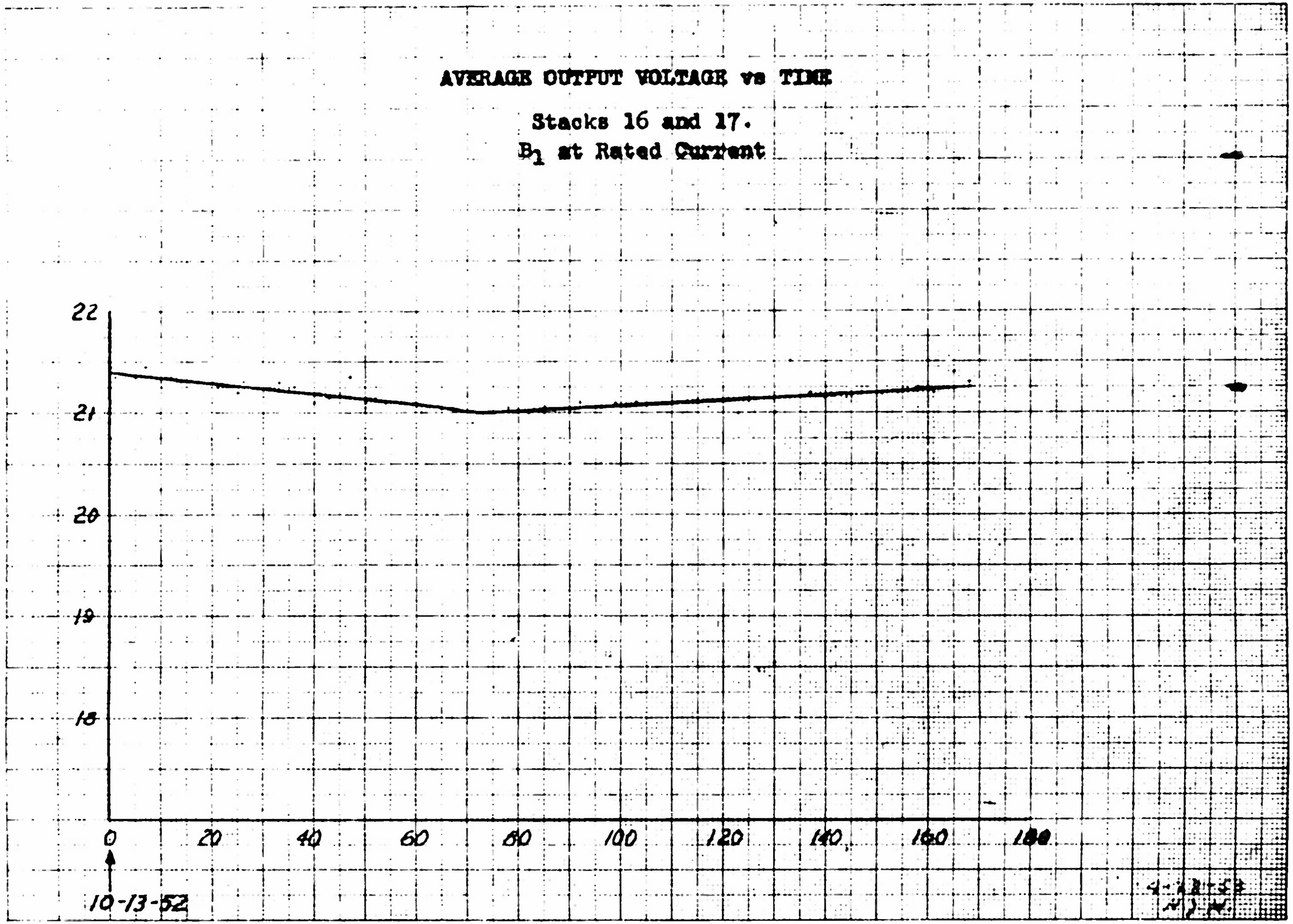

AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 50, 51, and 53.
B1 at Rated Current
22
21
20
19
18
D.C. Output - Volts
0
20
40
60
80
Time - Days
1-13-53

Fig. 5



AVERAGE OUTPUT VOLTAGE vs TIME
Stacks 16 and 17.
B1 at Rated Current
22
21
20
19
18
0
20
40
60
80
100
120
140
160
180
10-13-52

Fig. 6

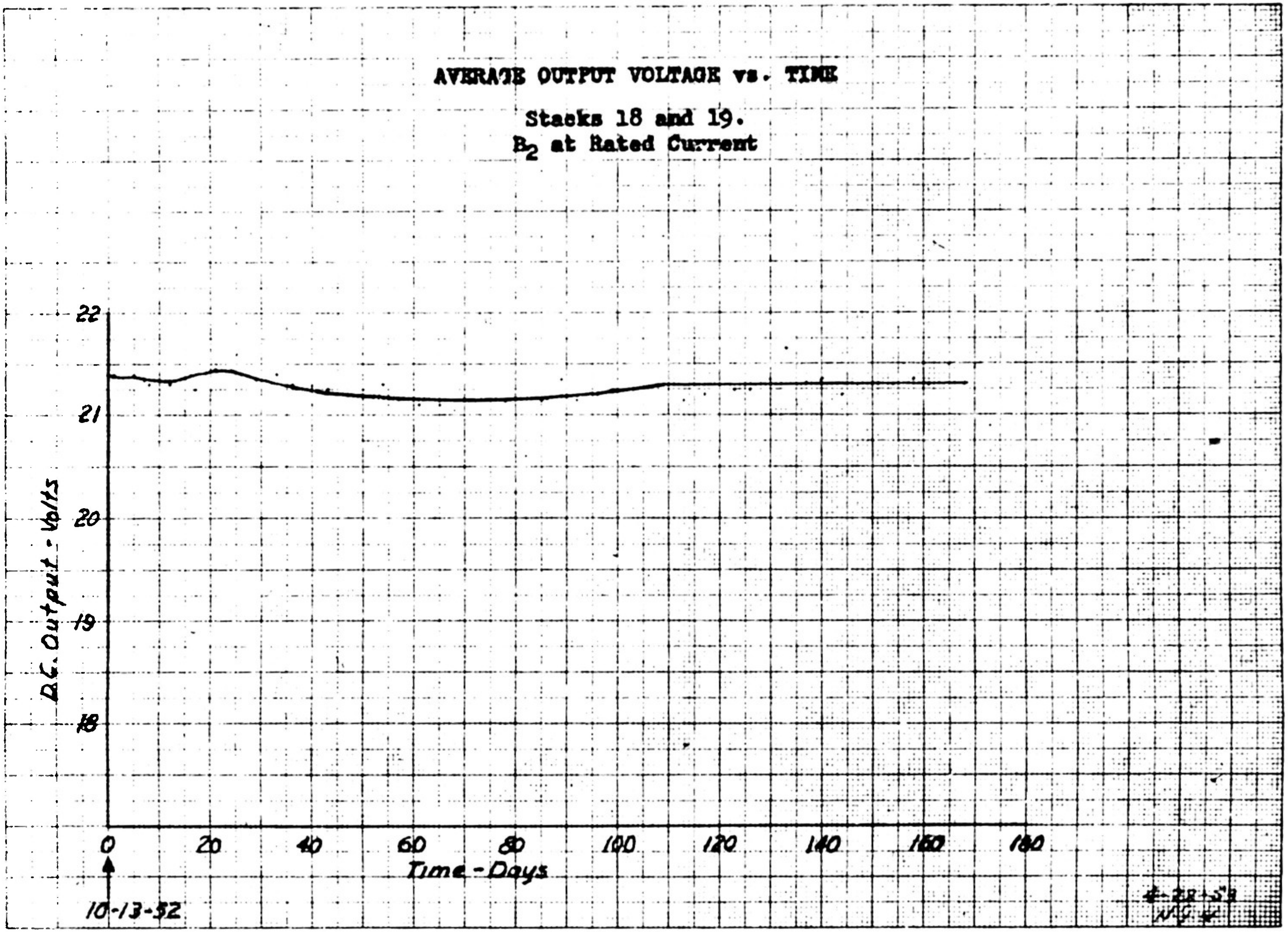
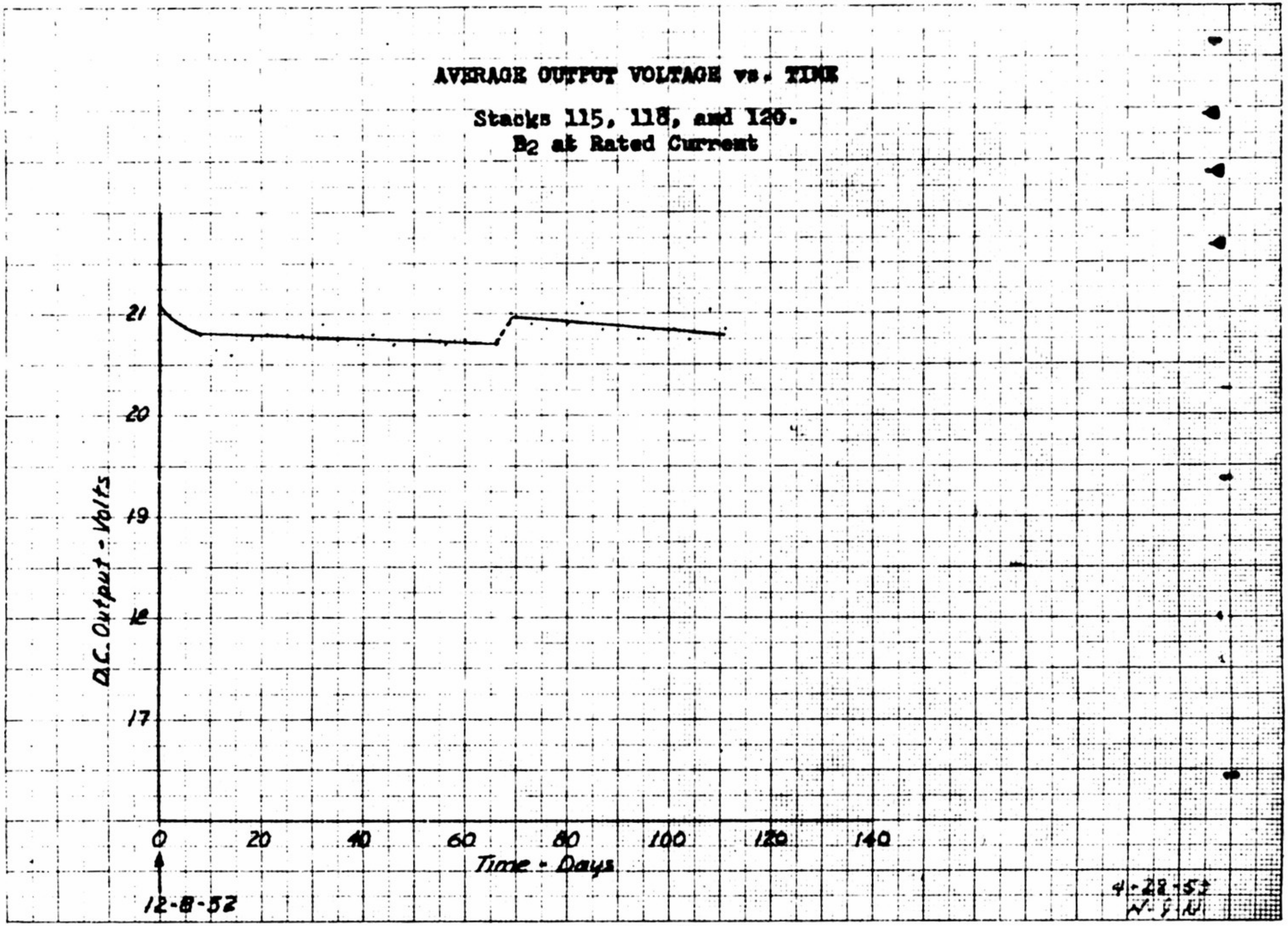

AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 18 and 19.
B_2 at Rated Current
22
21
20
19
18
D.C. Output - Volts
0
20
40
60
80
100
120
140
160
180
Time - Days
10-13-52

Fig. 7



AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 115, 118, and 120.
B_2 at Rated Current
D.C. Output - Volts
21
20
19
18
17
0
20
40
60
80
100
120
140
Time - Days
12-8-52
4-28-53

Fig. 8

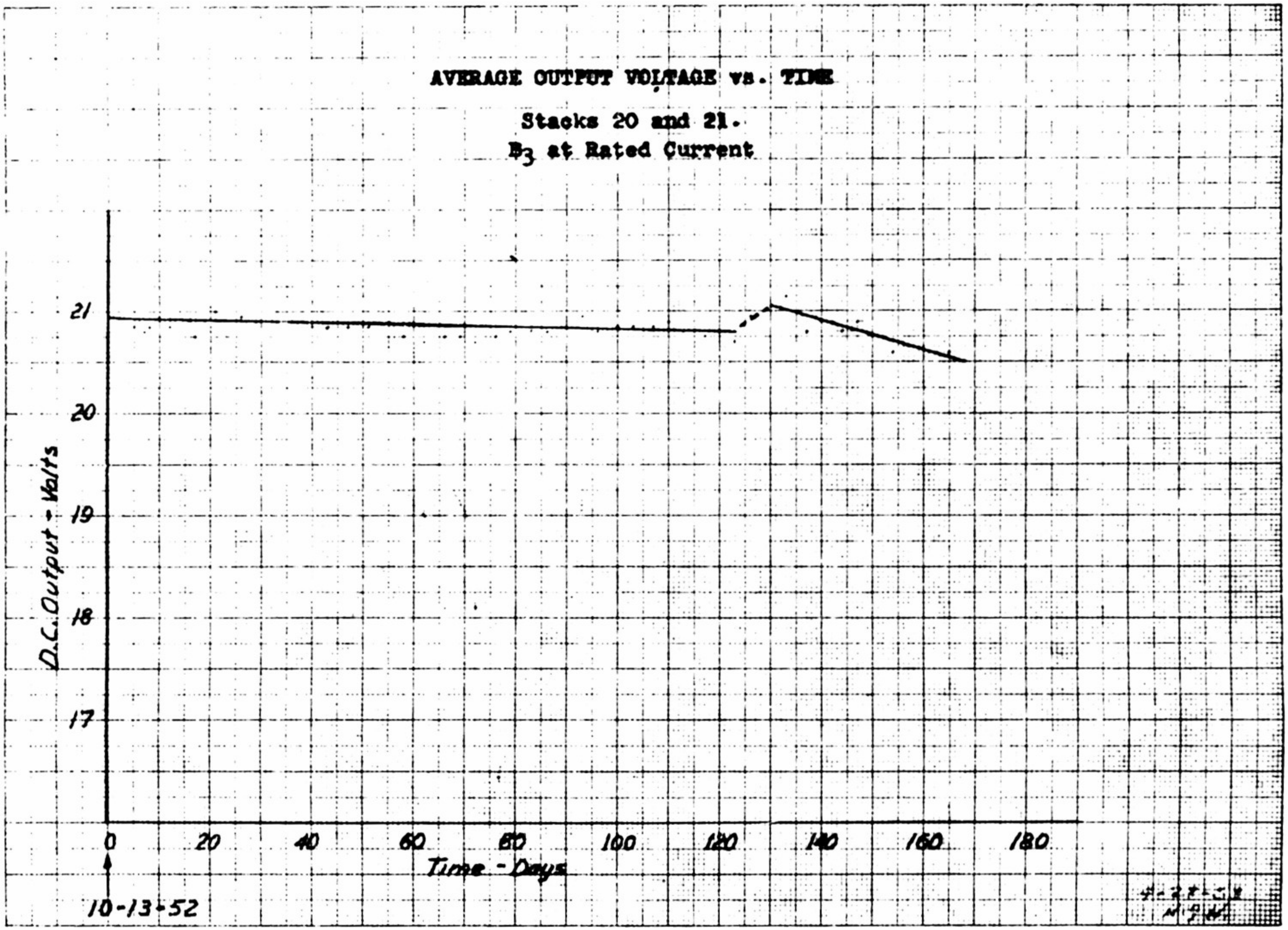
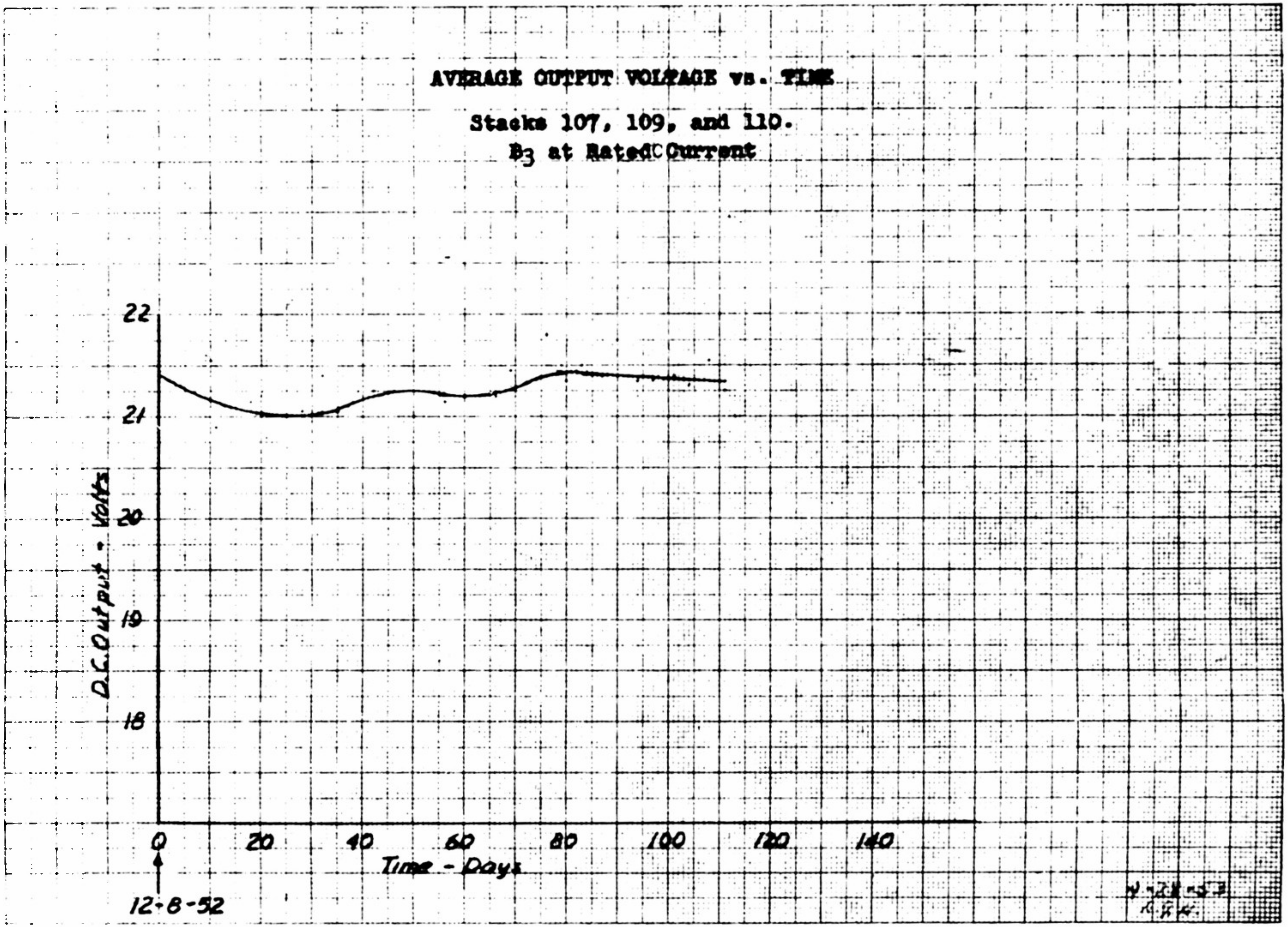

AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 20 and 21.
B_3 at Rated Current
D.C. Output - Volts
21
20
19
18
17
0
20
40
60
80
100
120
140
160
180
Time - Days
10-13-52

Fig. 9



AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 107, 109, and 110.
B3 at Rated Current
22
21
20
19
18
D.C. Output - Volts
0
20
40
60
80
100
120
140
Time - Days
12-8-52

Fig. 10

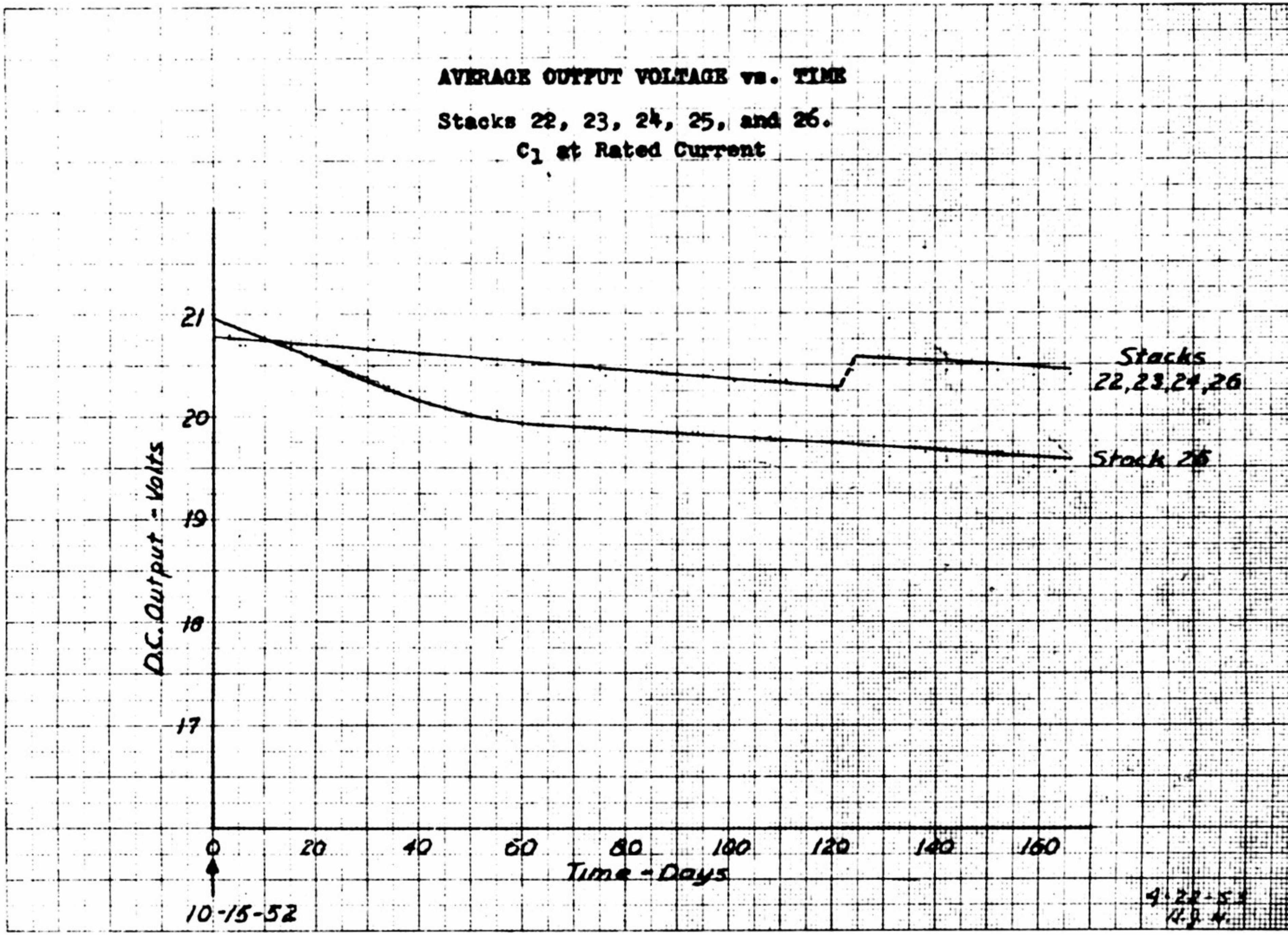

AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 22, 23, 24, 25, and 26.
C_1 at Rated Current
21
20
19
18
17
D.C. Output - Volts
0
20
40
60
80
100
120
140
160
Time - Days
10-15-52
Stacks 22,23,24,26
Stack 25

Fig. 11

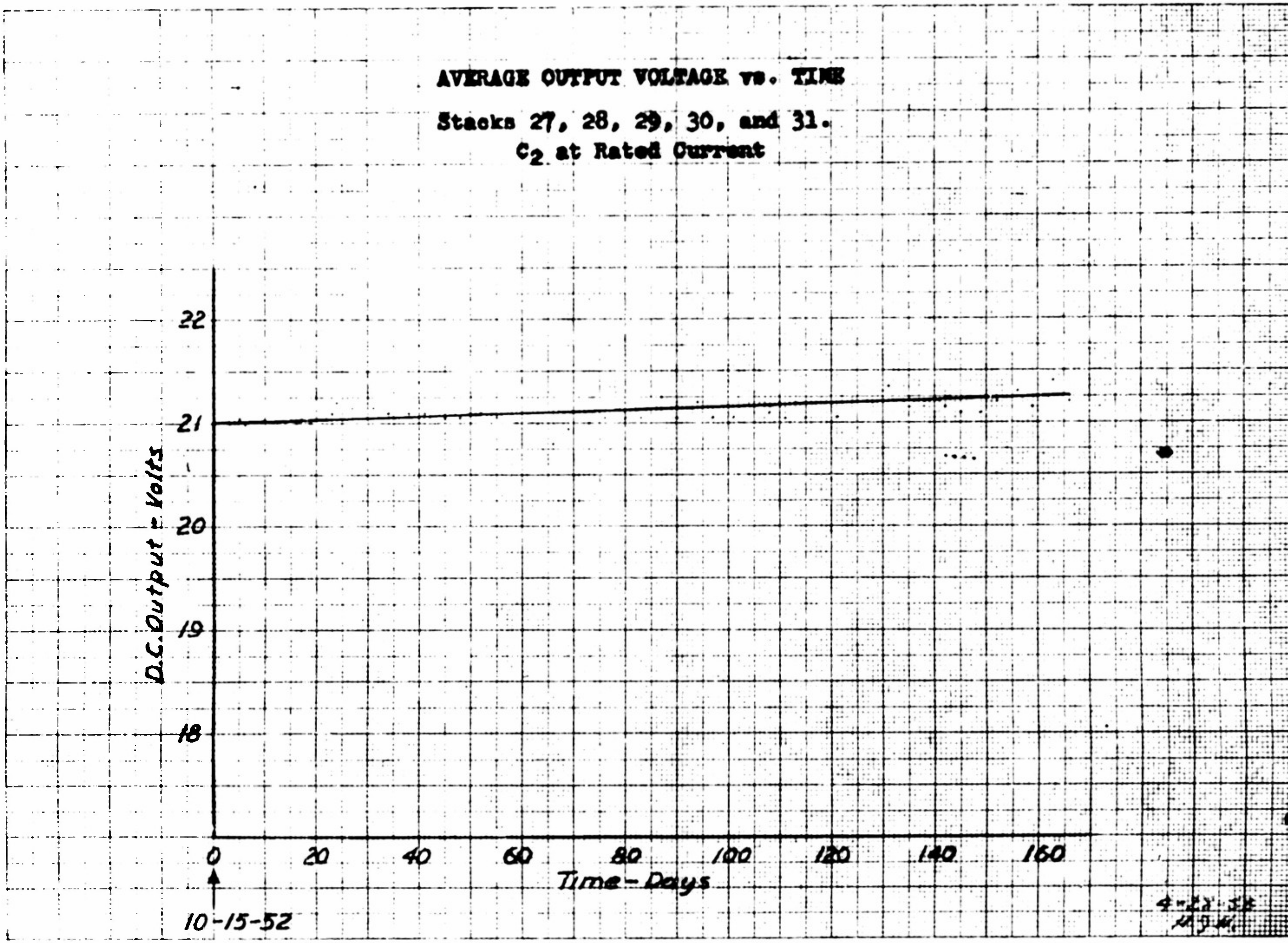

AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 27, 28, 29, 30, and 31.
C_2 at Rated Current
D.C. Output = Volts
22
21
20
19
18
0
20
40
60
80
100
120
140
160
Time-Days
10-15-52

Fig. 12

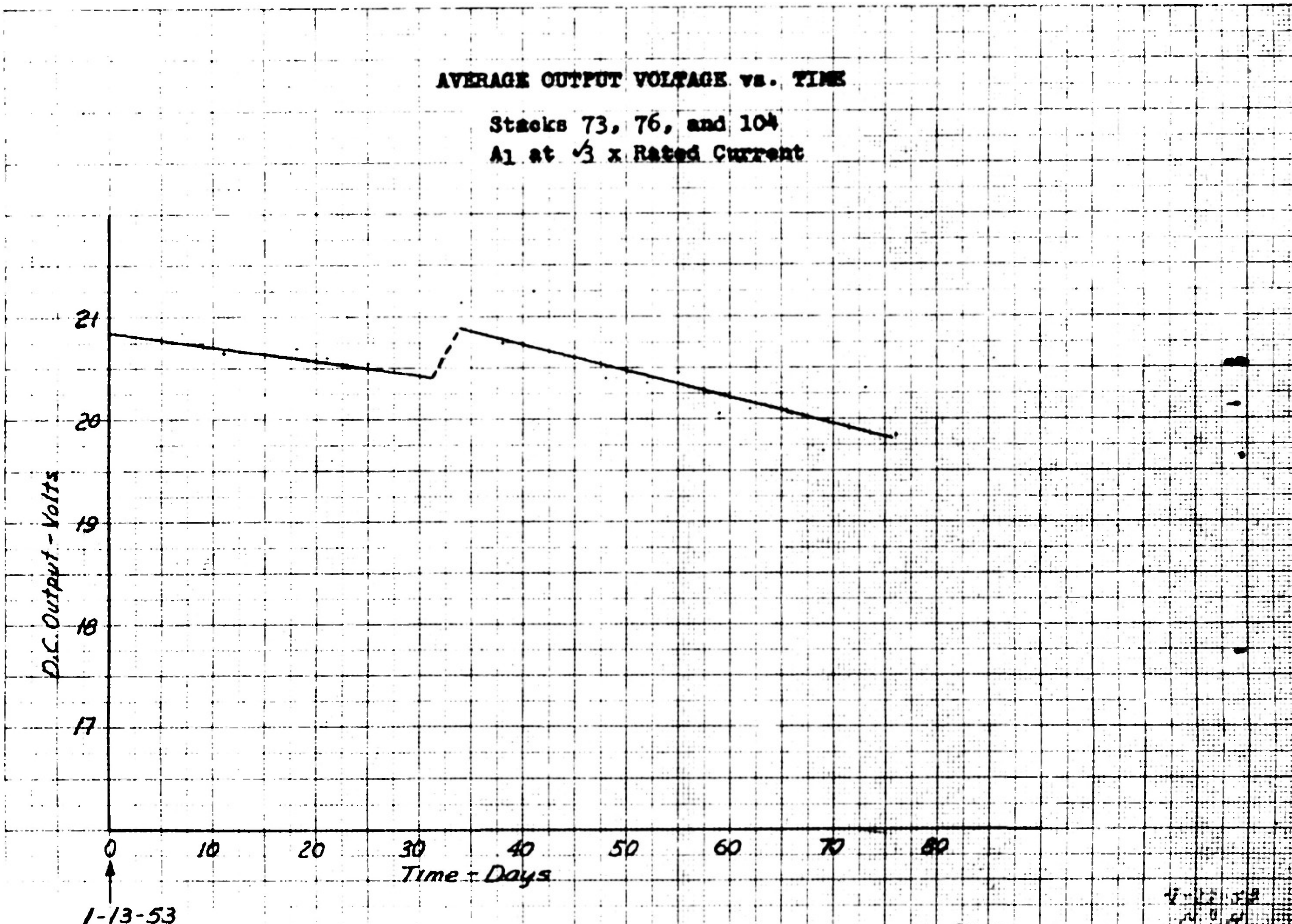
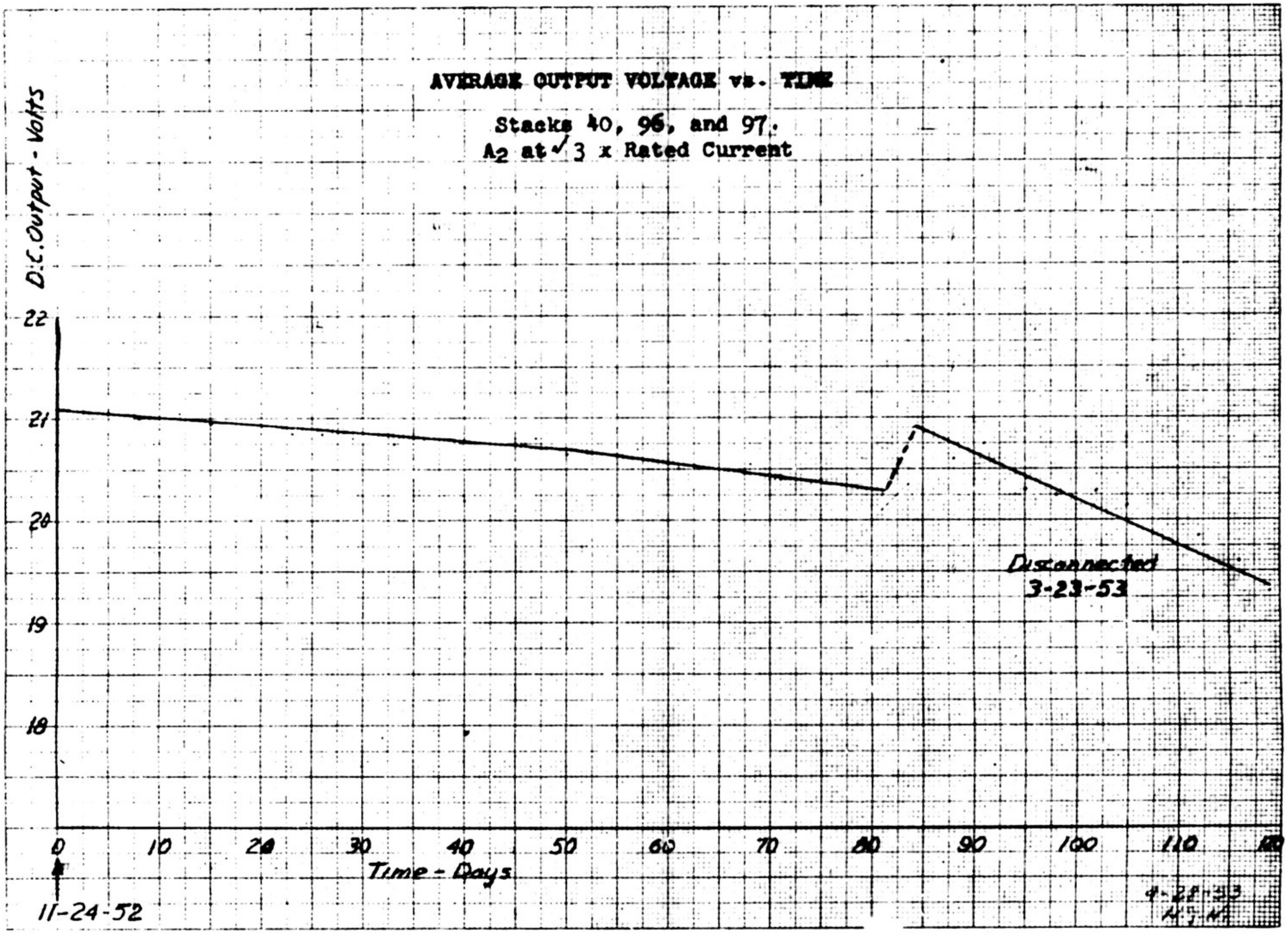

AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 73, 76, and 104
A_1 at $\sqrt{3}$ x Rated Current
21
20
19
18
17
D.C. Output - Volts
0
10
20
30
40
50
60
70
80
Time - Days
1-13-53

Fig. 13



AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 40, 96, and 97.
A_2 at $\sqrt{3}$ x Rated Current
D.C. Output - Volts
22
21
20
19
18
0
10
20
30
40
50
60
70
80
90
100
110
120
Time - Days
11-24-52
Disconnected
3-23-53

Fig. 14

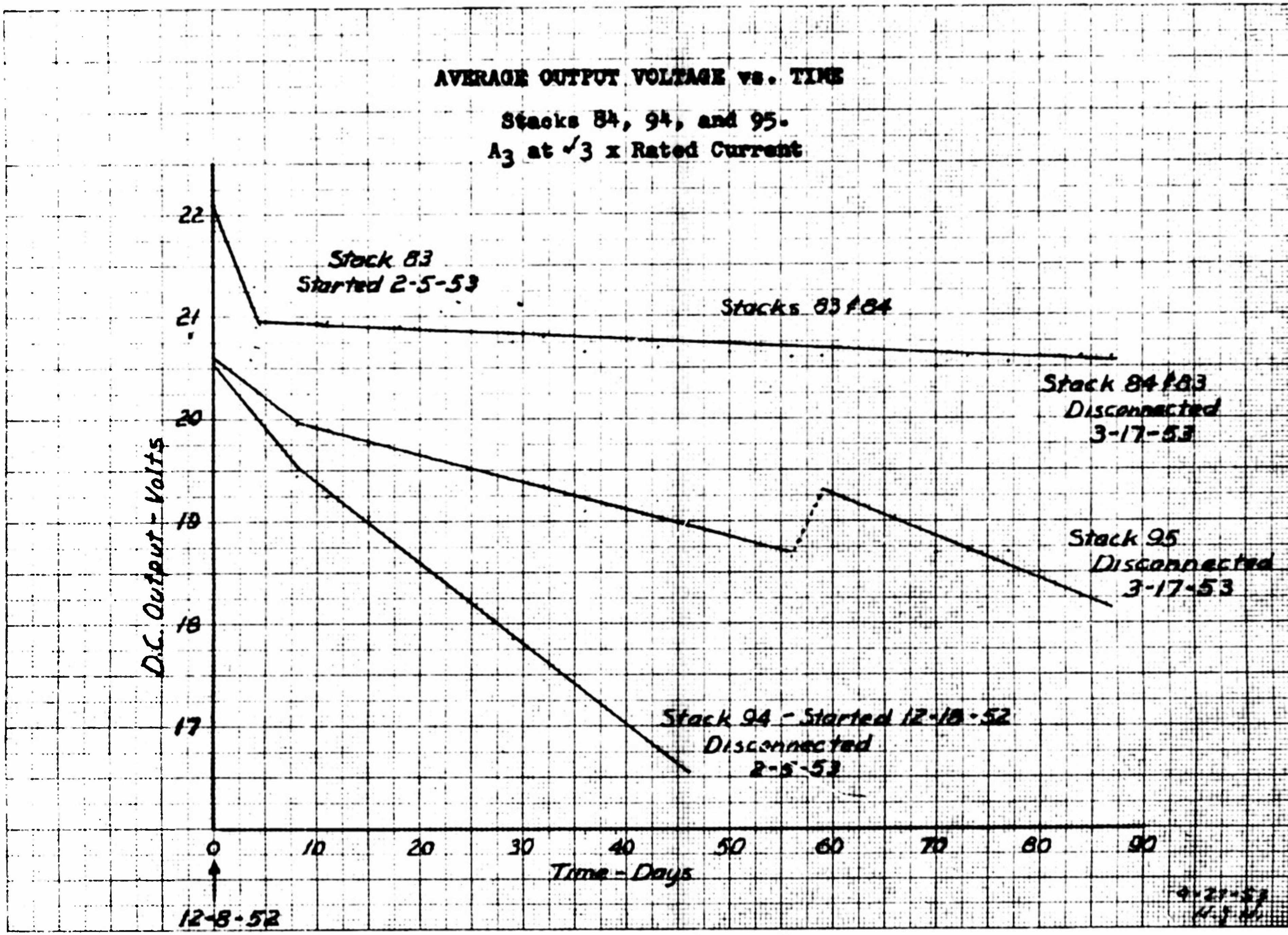

AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 84, 94, and 95.
A_3 at $\sqrt{3}$ x Rated Current
Stack 83
Started 2-5-53
Stacks 83 & 84
Stack 84 & 83
Disconnected
3-17-53
Stack 95
Disconnected
3-17-53
Stack 94 - Started 12-18-52
Disconnected
2-5-53
D.C. Output - Volts
22
21
20
19
18
17
0
10
20
30
40
50
60
70
80
90
Time - Days
12-8-52

Fig. 15

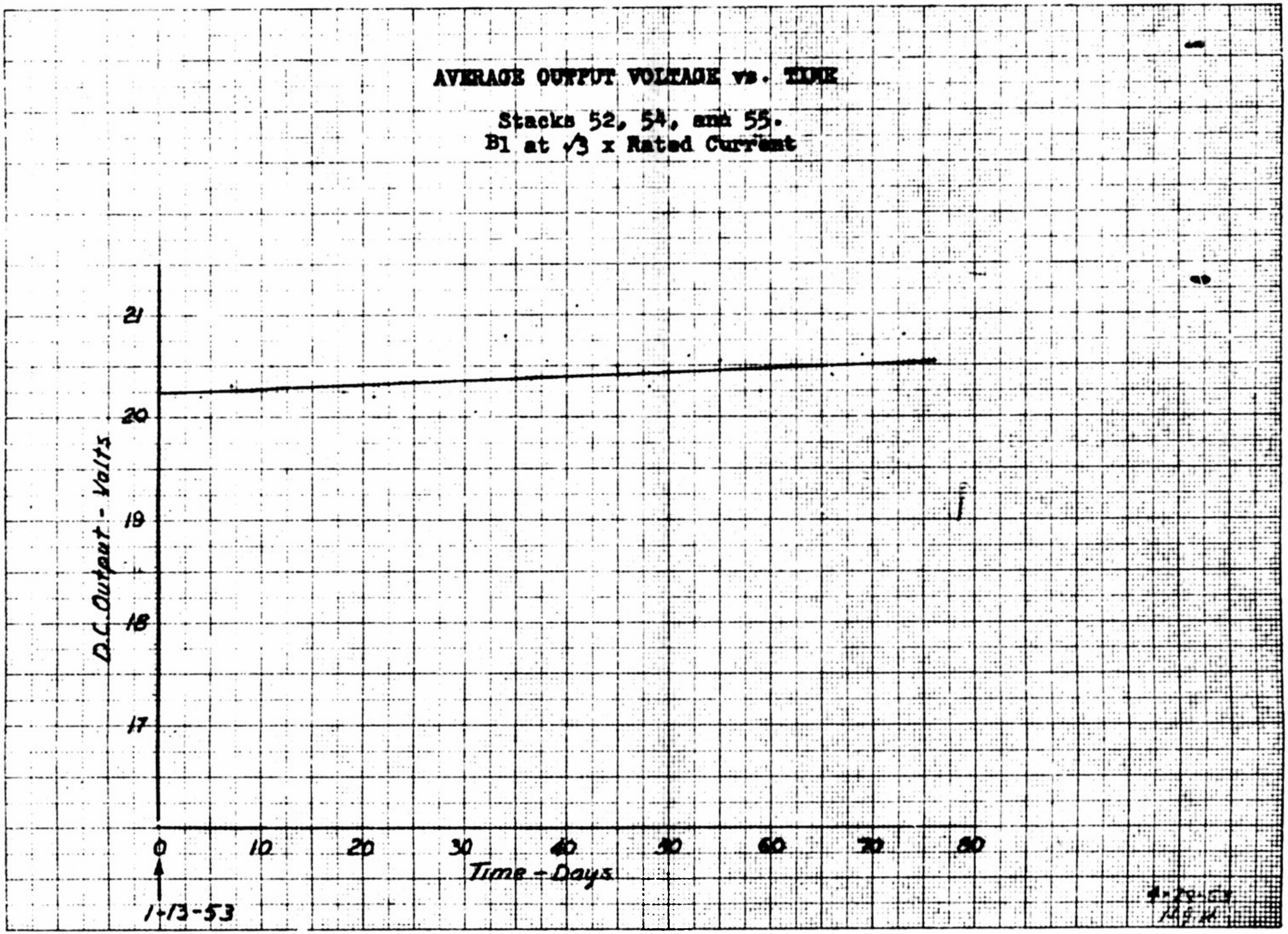

AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 52, 54, and 55.
B1 at √3 x Rated Current
D.C. Output - Volts
21
20
19
18
17
0
10
20
30
40
50
60
70
80
Time - Days
1-13-53

Fig. 16

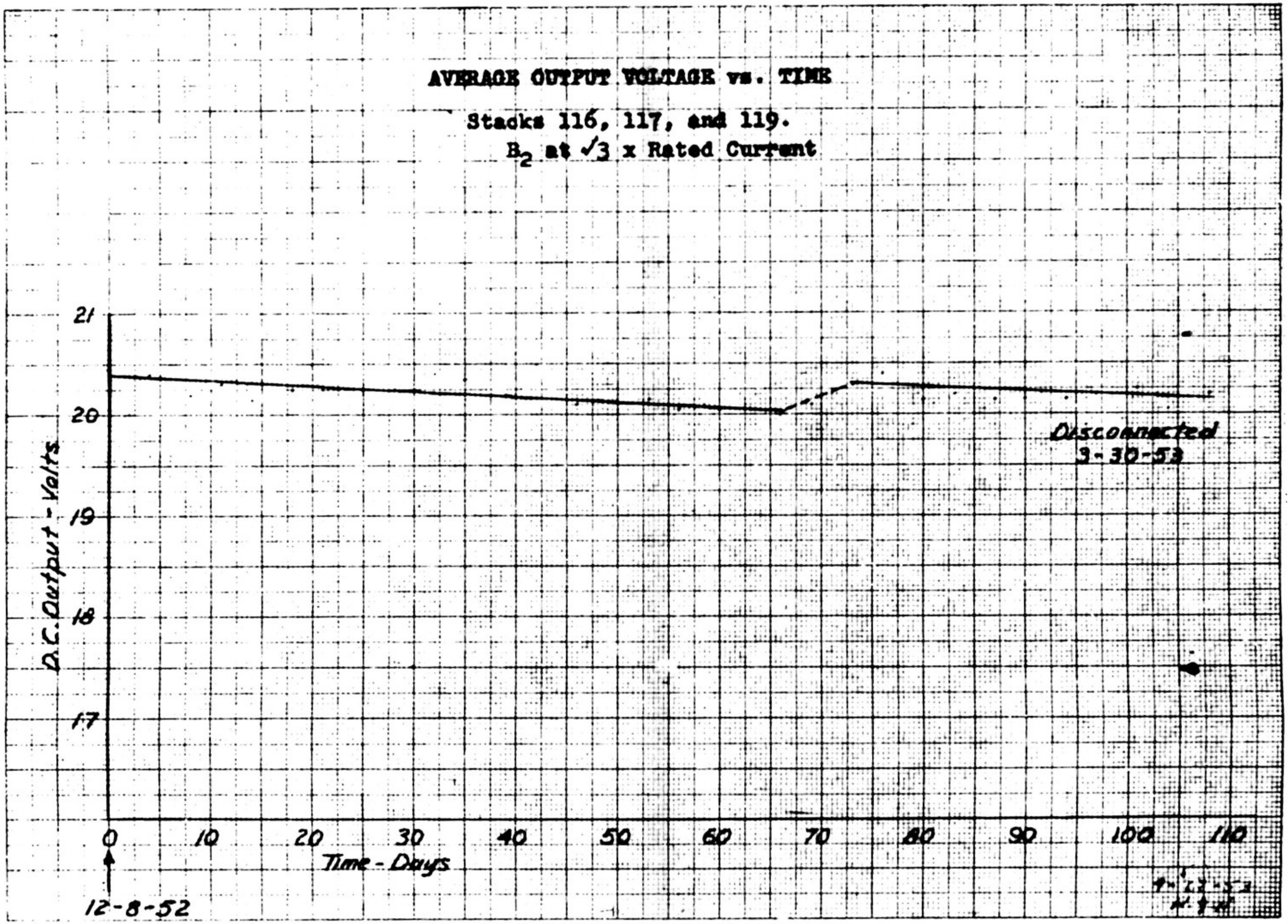
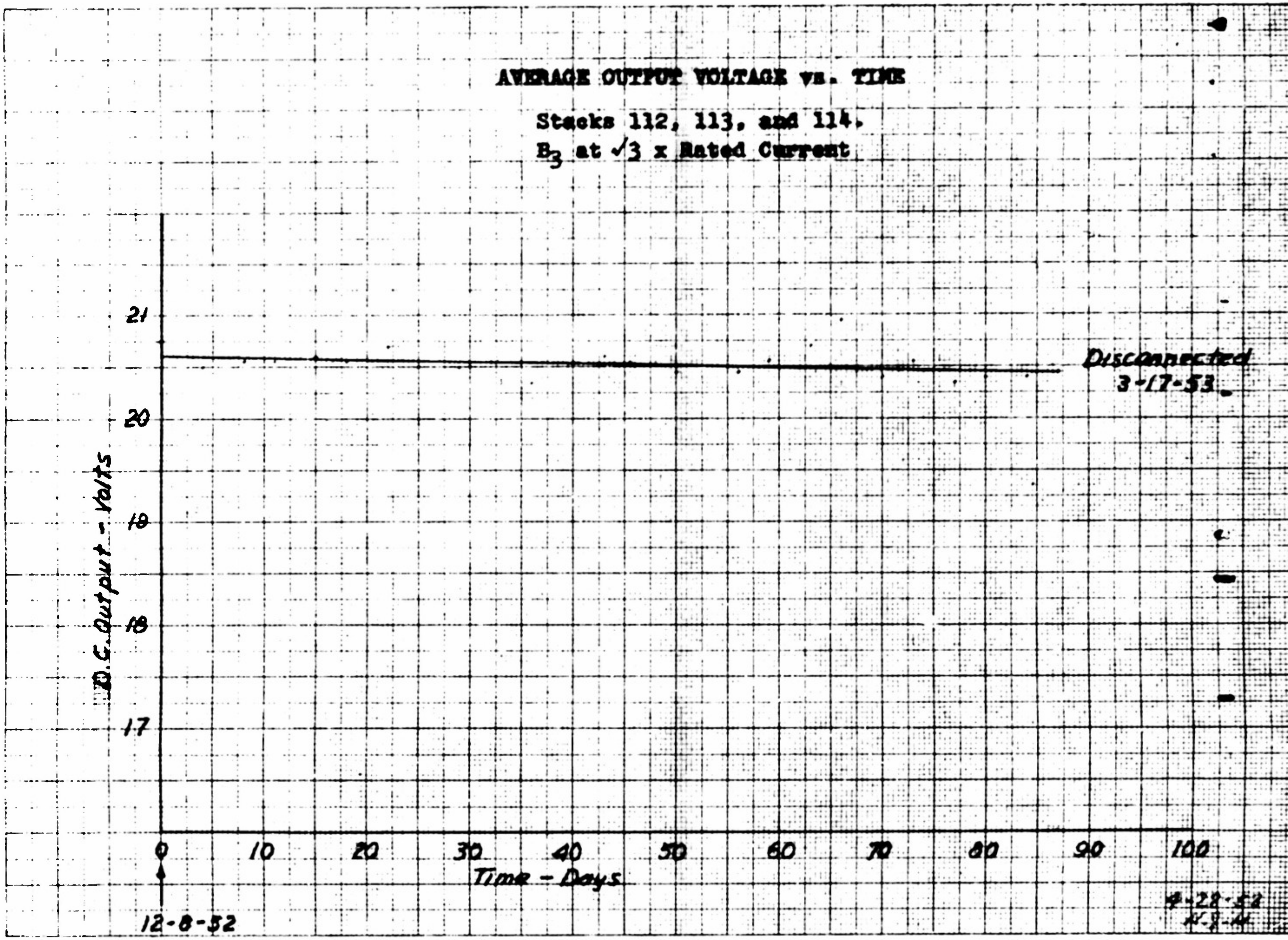

AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 116, 117, and 119.
B_2 at $\sqrt{3}$ x Rated Current
D.C. Output - Volts
21
20
19
18
17
0
10
20
30
40
50
60
70
80
90
100
110
Time - Days
12-8-52
Disconnected
3-30-53

Fig. 17



AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 112, 113, and 114.
B3 at √3 x Rated Current
Disconnected
3-17-53
D.C. Output - Volts
21
20
19
18
17
0
10
20
30
40
50
60
70
80
90
100
Time - Days
12-8-52

Fig. 18

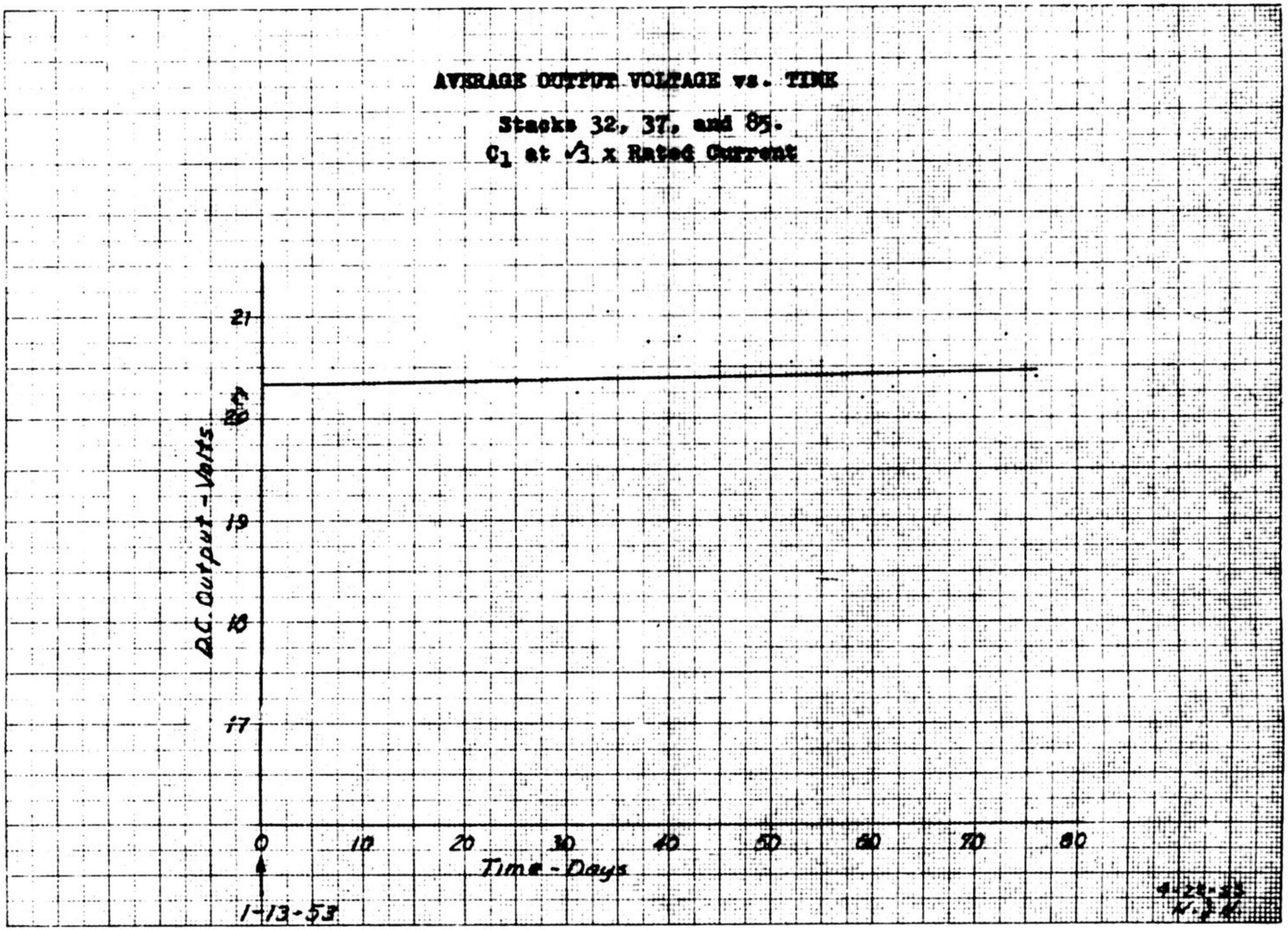

AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 32, 37, and 85.
C_1 at $\sqrt{3}$ x Rated Current
D.C. Output - Volts
21
20
19
18
17
0
10
20
30
40
50
60
70
80
Time - Days
1-13-53
4-28-53

Fig. 19

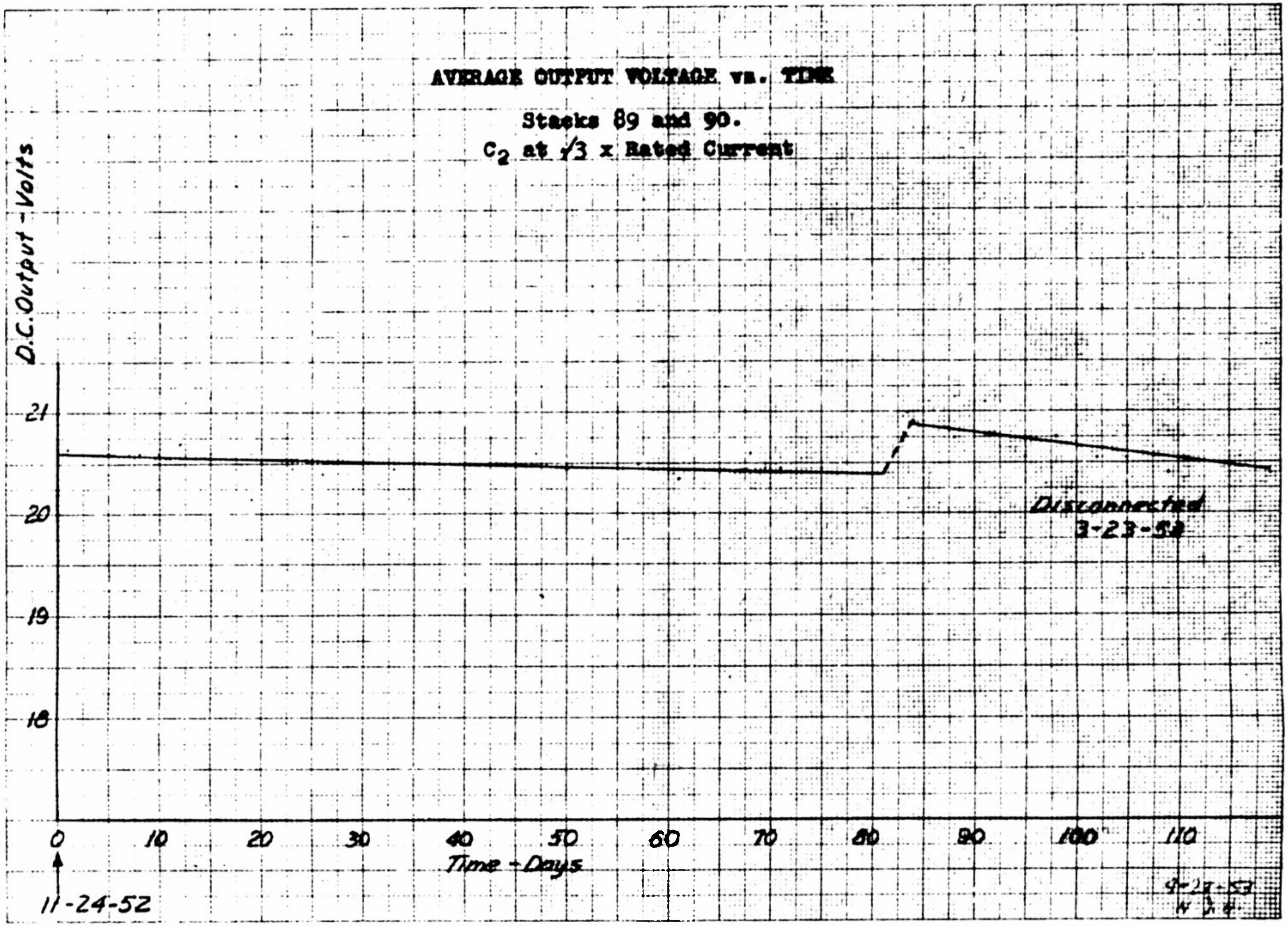
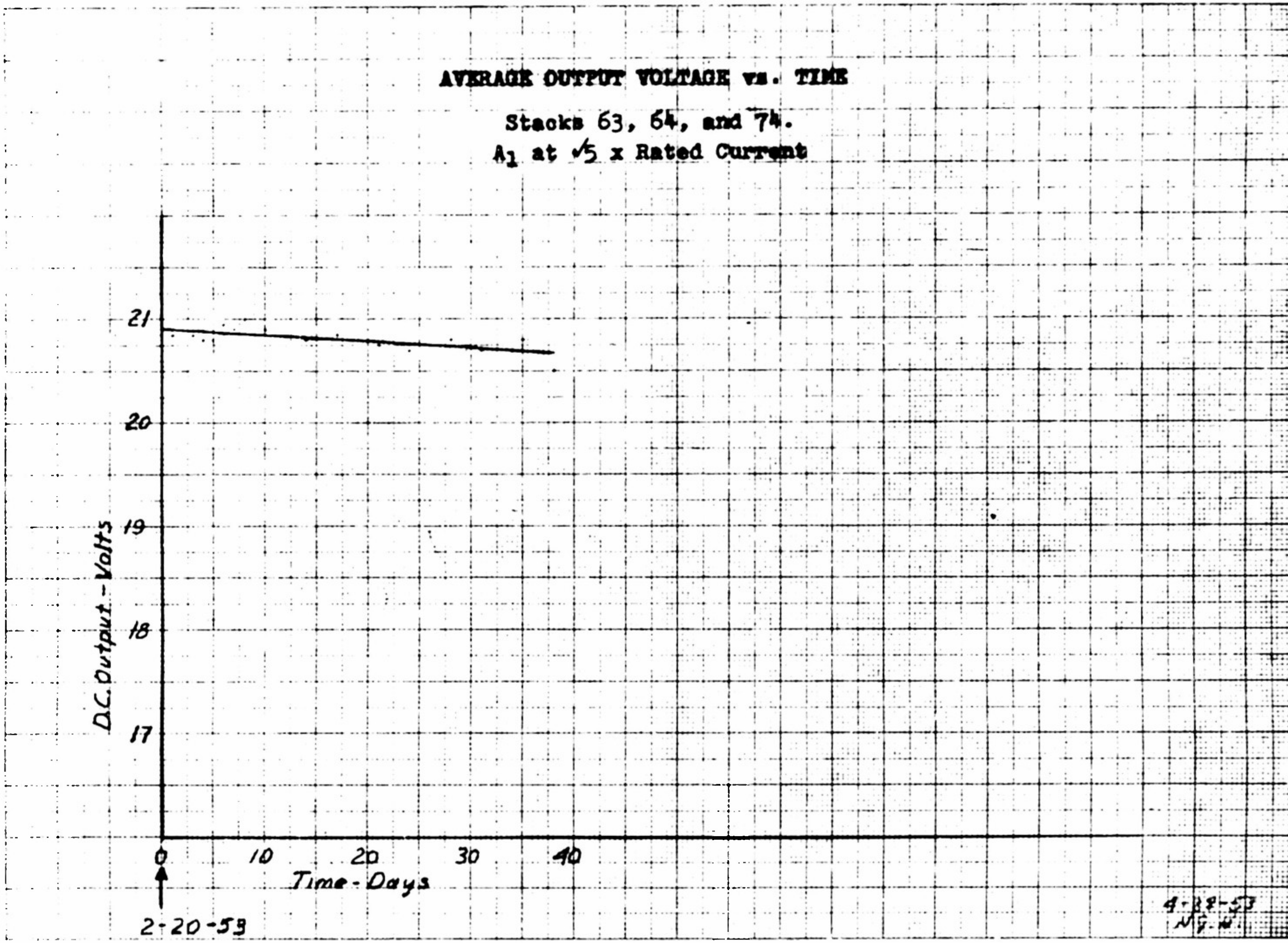

AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 89 and 90.
C2 at √3 x Rated Current
D.C. Output - Volts
21
20
19
18
0
10
20
30
40
50
60
70
80
90
100
110
Time - Days
11-24-52
Disconnected
3-23-53

Fig. 20



AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 63, 64, and 74.
A_1 at $\sqrt{5}$ x Rated Current
D.C. Output - Volts
21
20
19
18
17
0
10
20
30
40
Time - Days
2-20-53

Fig. 21

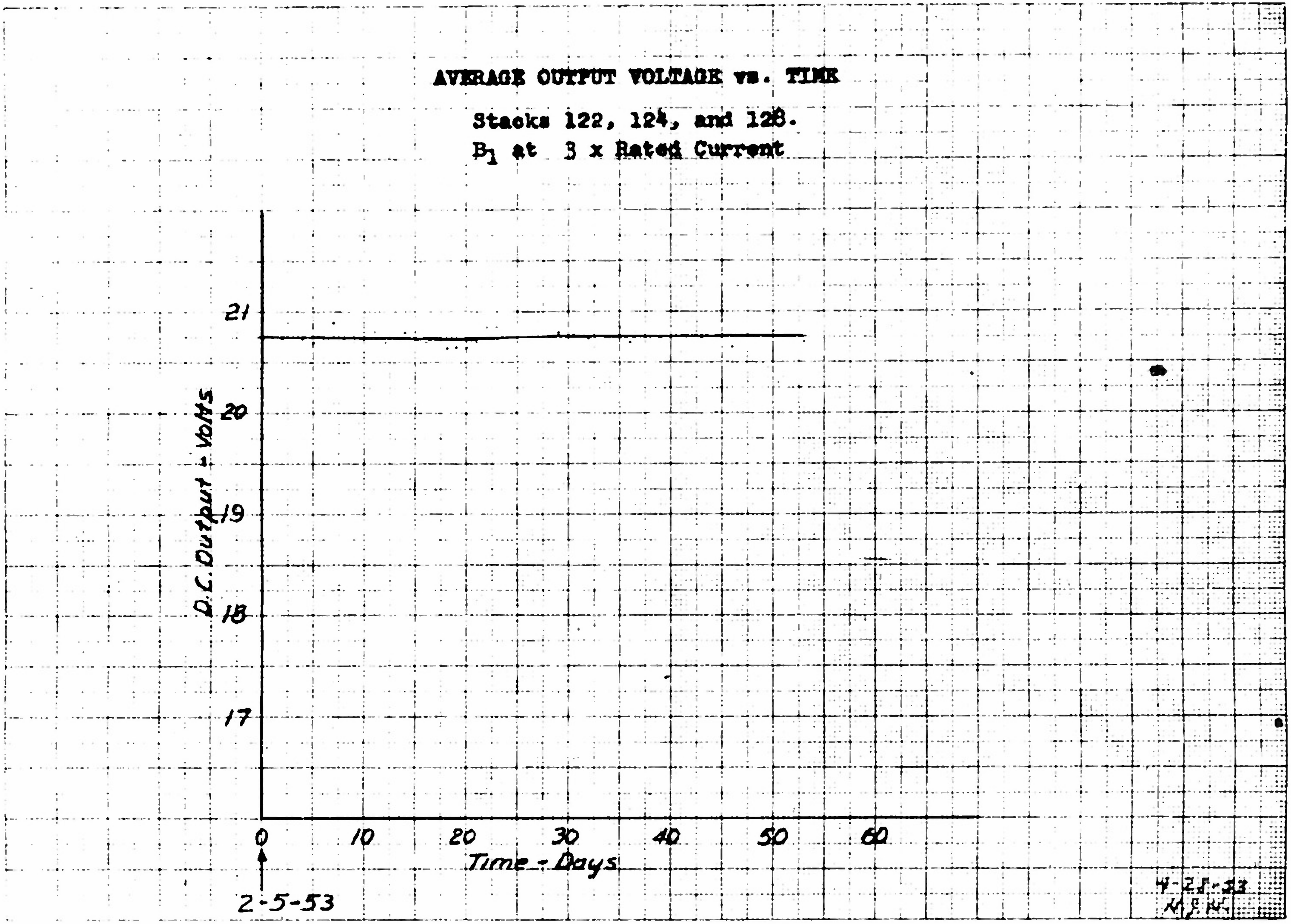
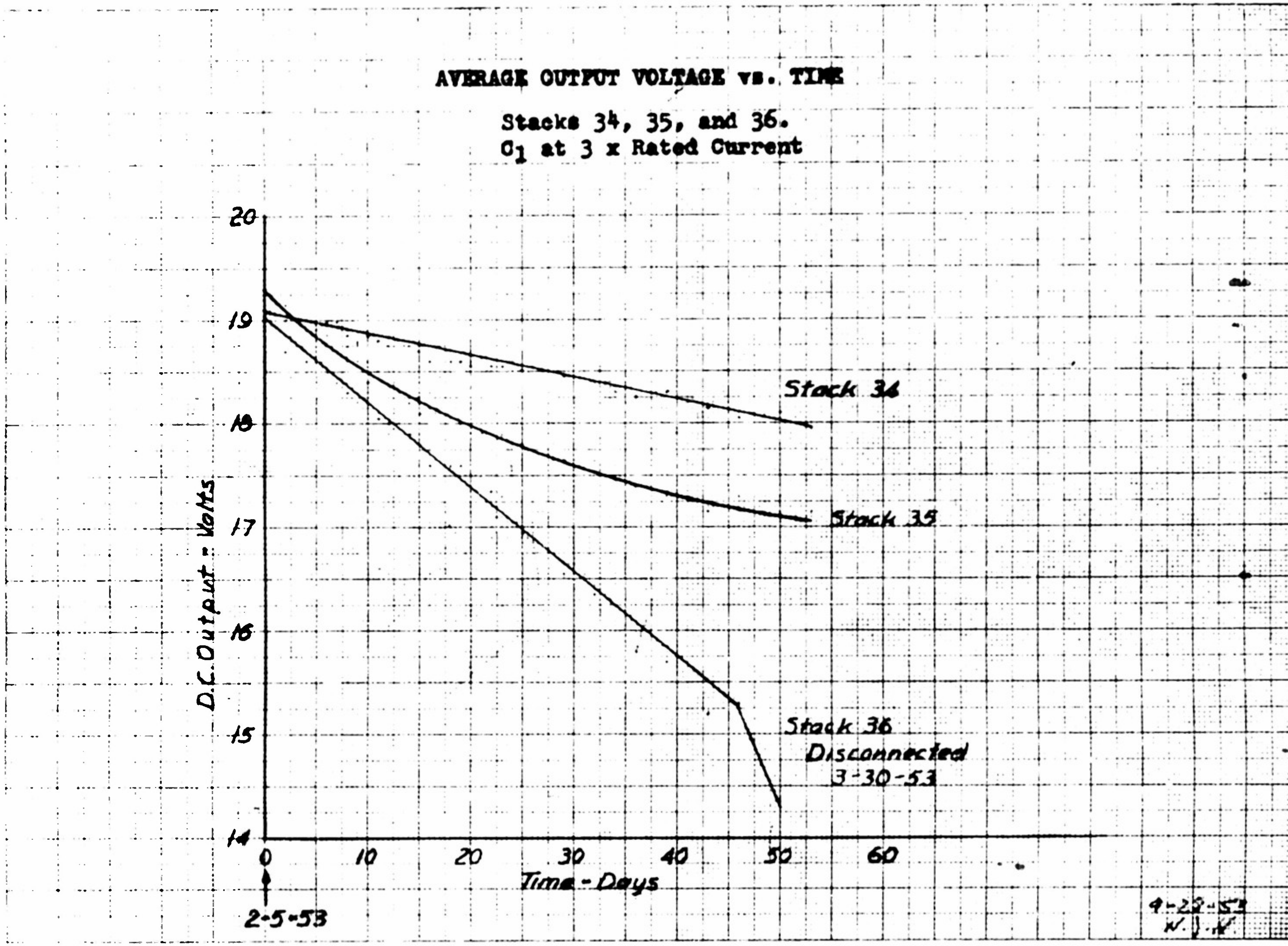
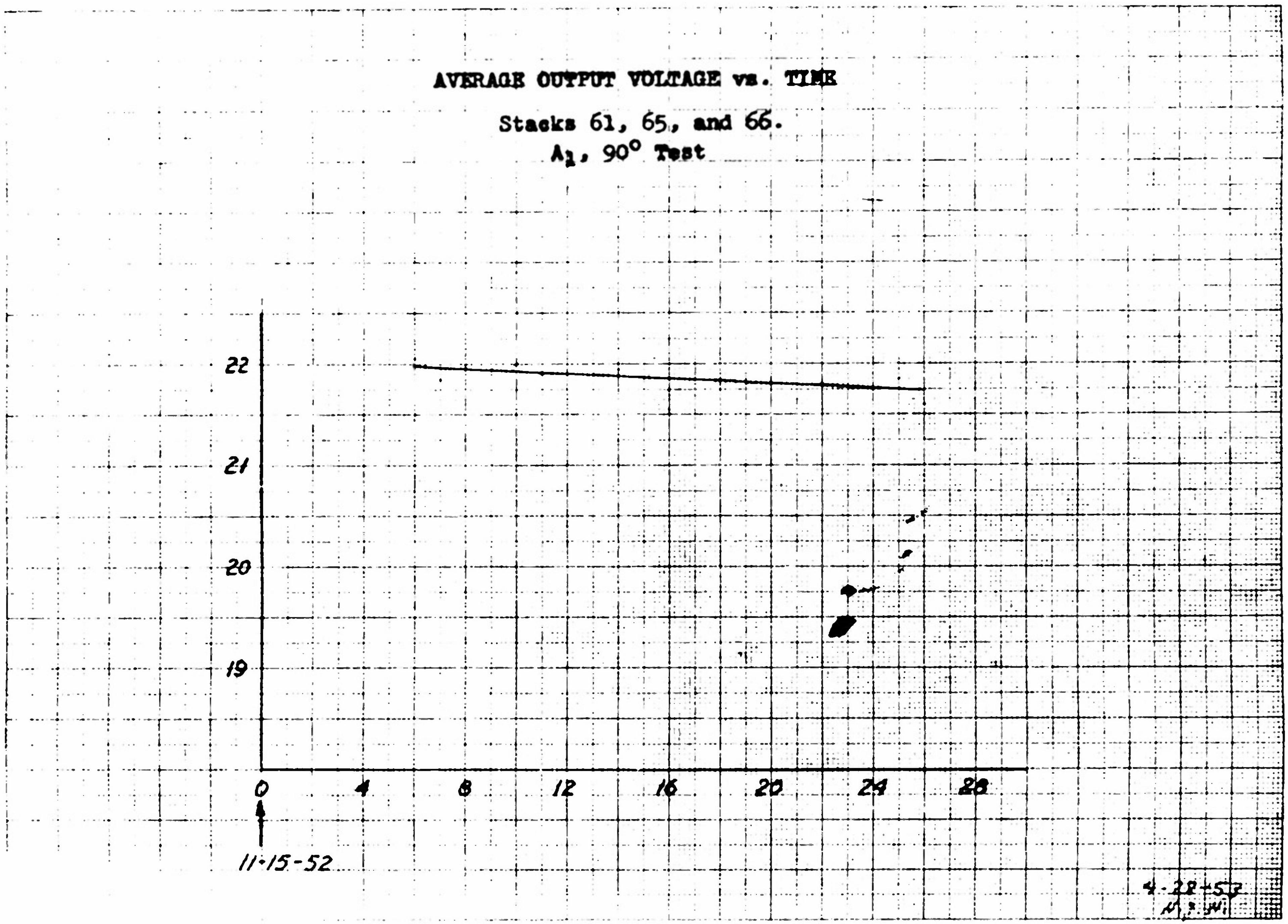

AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 122, 124, and 128.
B_1 at 3 x Rated Current
21
20
19
18
17
D.C. Output - Volts
0
10
20
30
40
50
60
Time - Days
2-5-53
4-25-53

Fig. 22



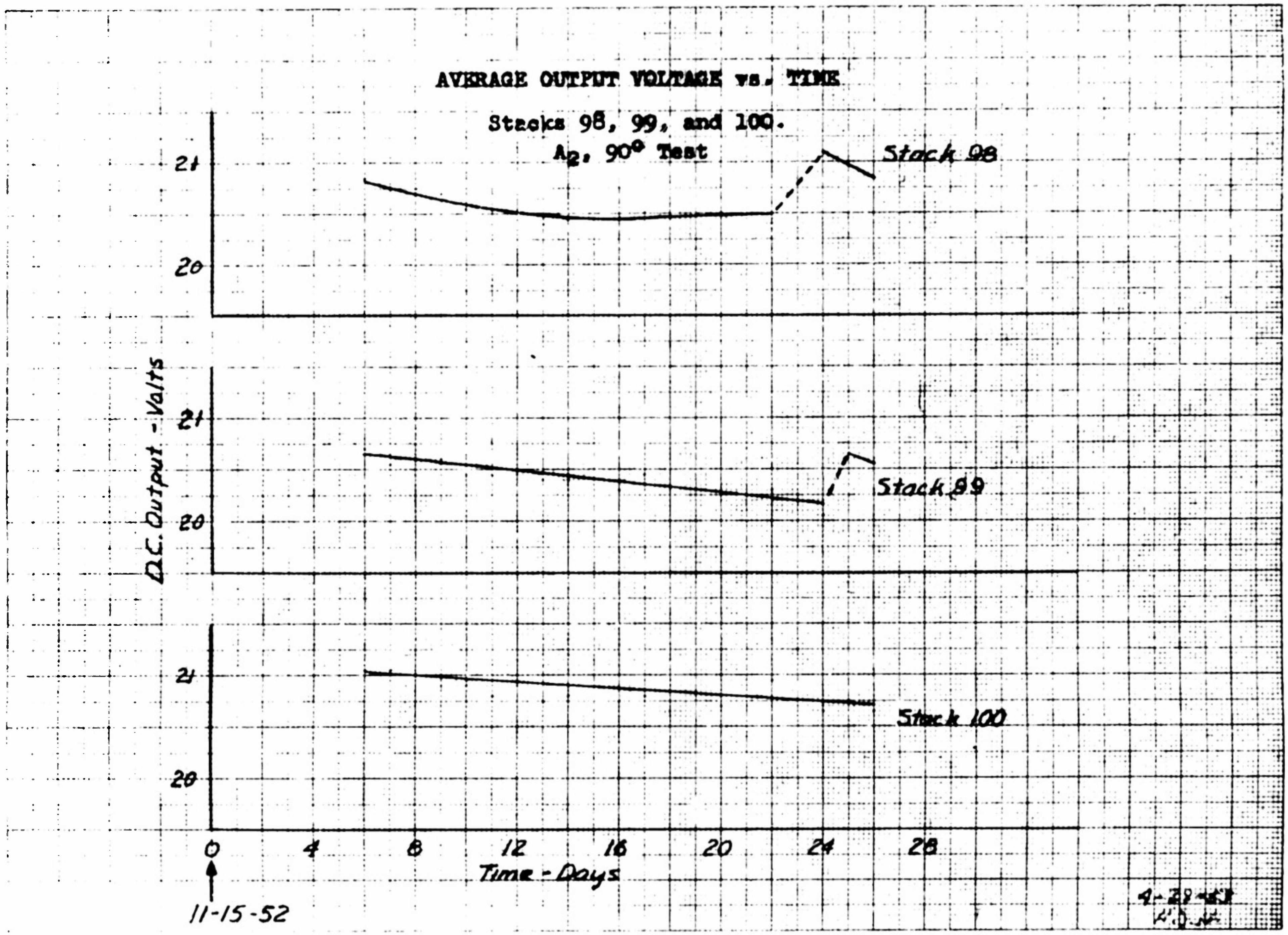
AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 34, 35, and 36.
C_1 at 3 x Rated Current
20
19
18
17
16
15
14
D.C. Output - Volts
0
10
20
30
40
50
60
Time - Days
2-5-53
Stack 34
Stack 35
Stack 36
Disconnected
3-30-53
4-23-53

Fig. 23



AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 61, 65, and 66.
A_1, 90° Test
22
21
20
19
0
4
8
12
16
20
24
28
11-15-52
4-22-53

Fig. 24



AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 98, 99, and 100.
A_2, 90° Test
Stack 98
Stack 99
Stack 100
D.C. Output - Volts
21
20
0
4
8
12
16
20
24
28
Time - Days
11-15-52

Fig. 25

AVERAGE OUTPUT VOLTAGE vs. TIME

Stacks 91, 92, and 93.
A_3, 90° Test

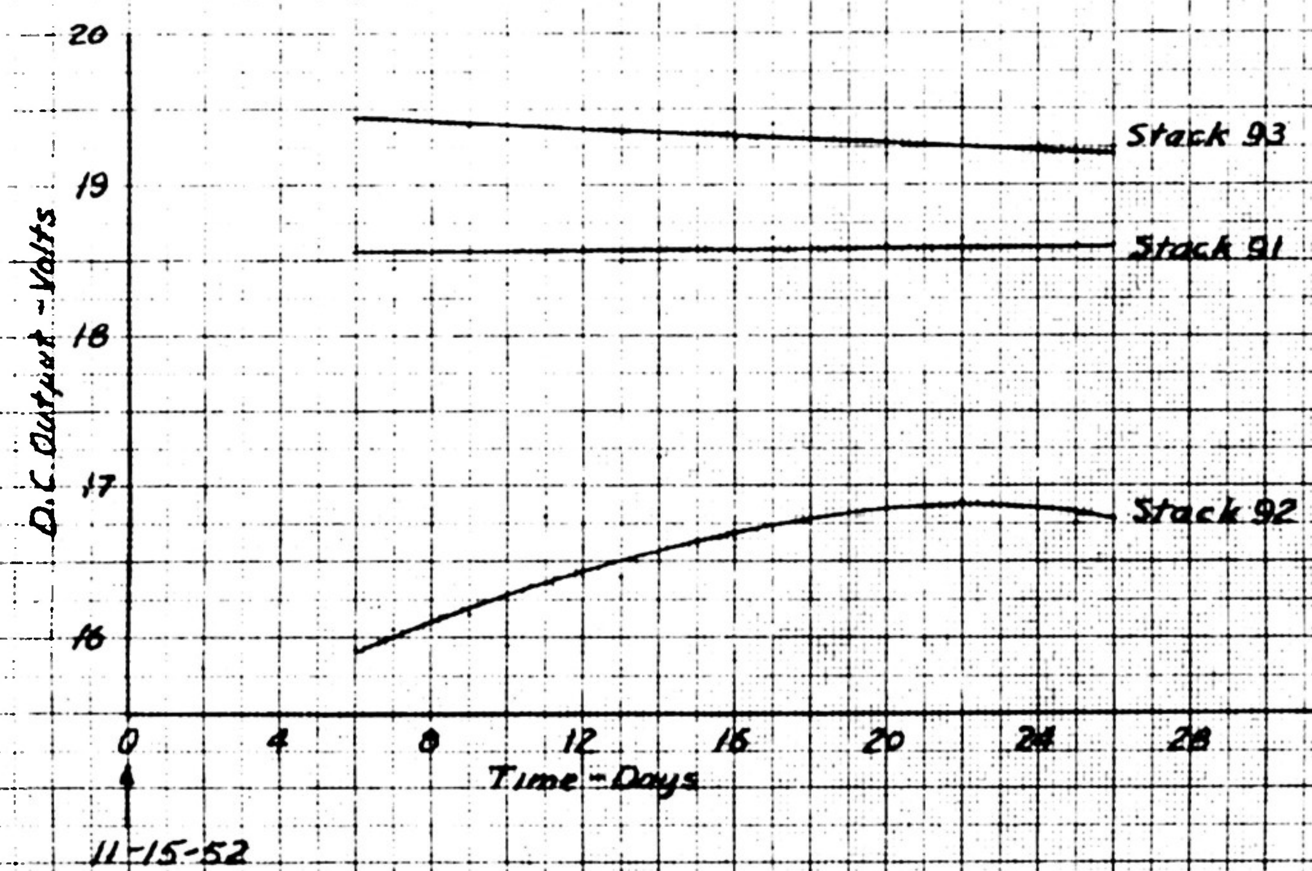


Fig. 26

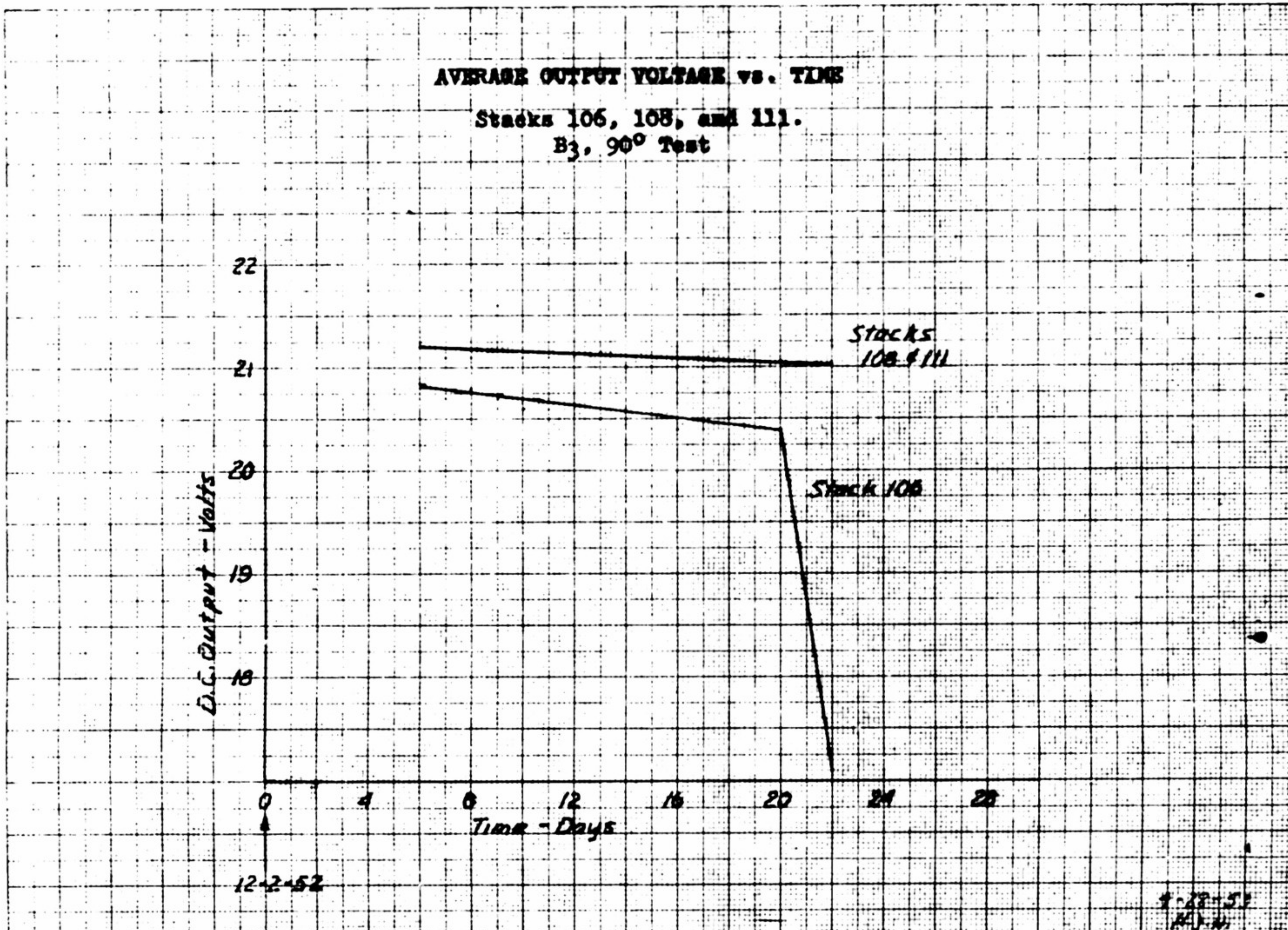

AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 106, 108, and 111.
B_3, 90° Test
22
21
20
19
18
D.C. Output - Volts
Stacks 108 & 111
Stack 106
0
4
8
12
16
20
24
28
Time - Days
12-2-52

Fig. 27

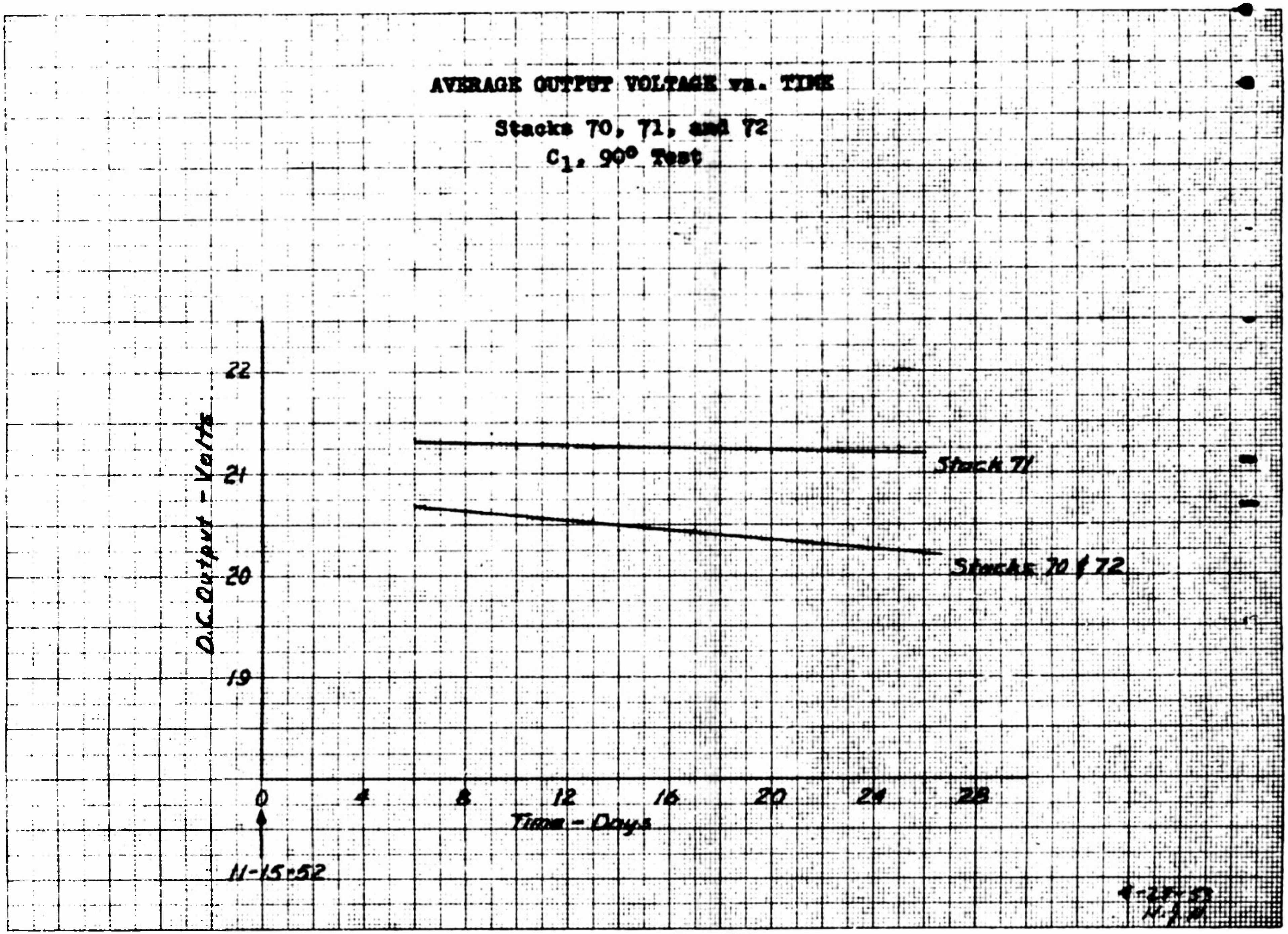

AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 70, 71, and 72
C_1, 90° Test
D.C. Output - Volts
22
21
20
19
0
4
8
12
16
20
24
28
Time - Days
11-15-52
Stack 71
Stacks 70 & 72

Fig. 28

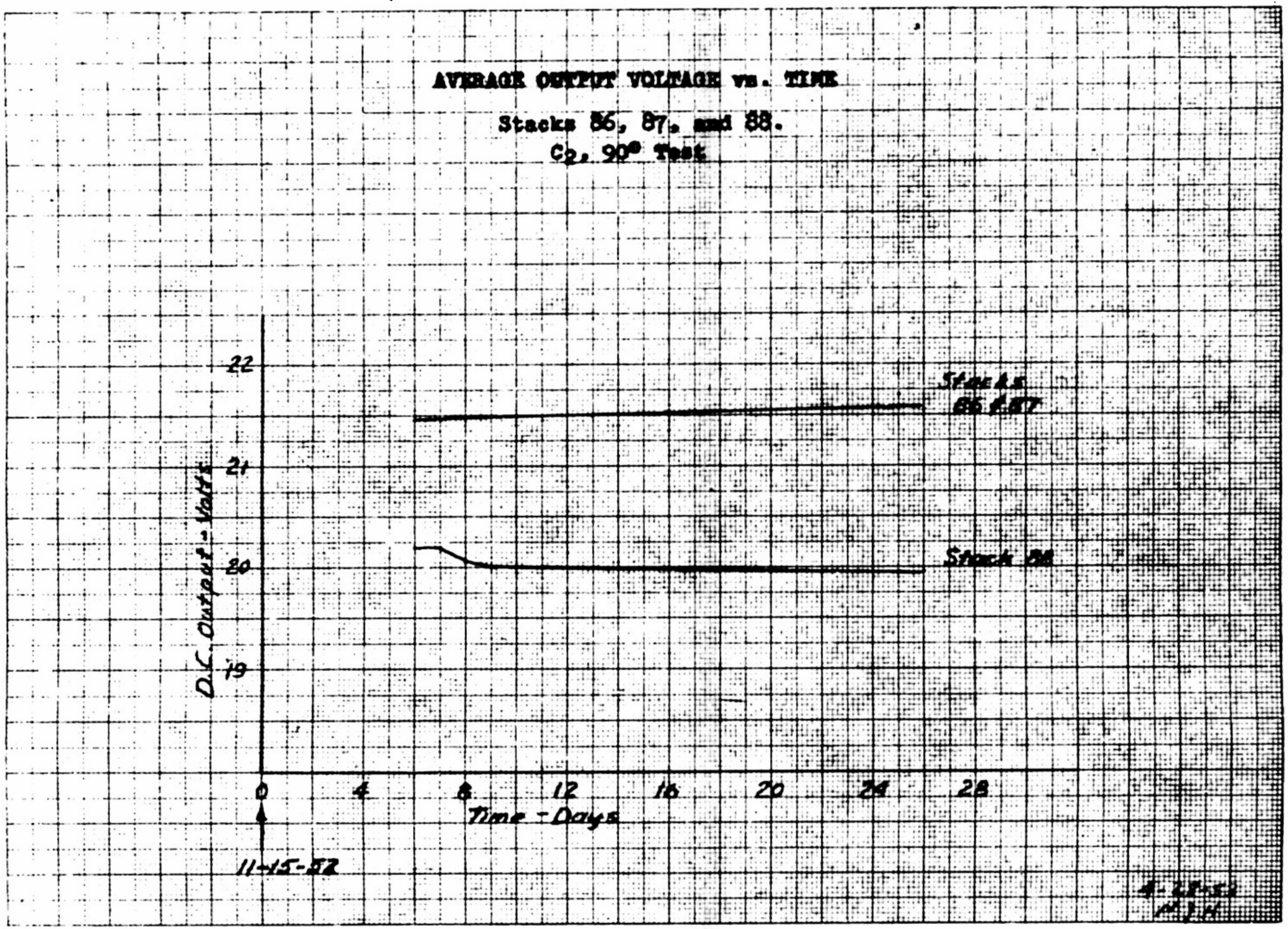
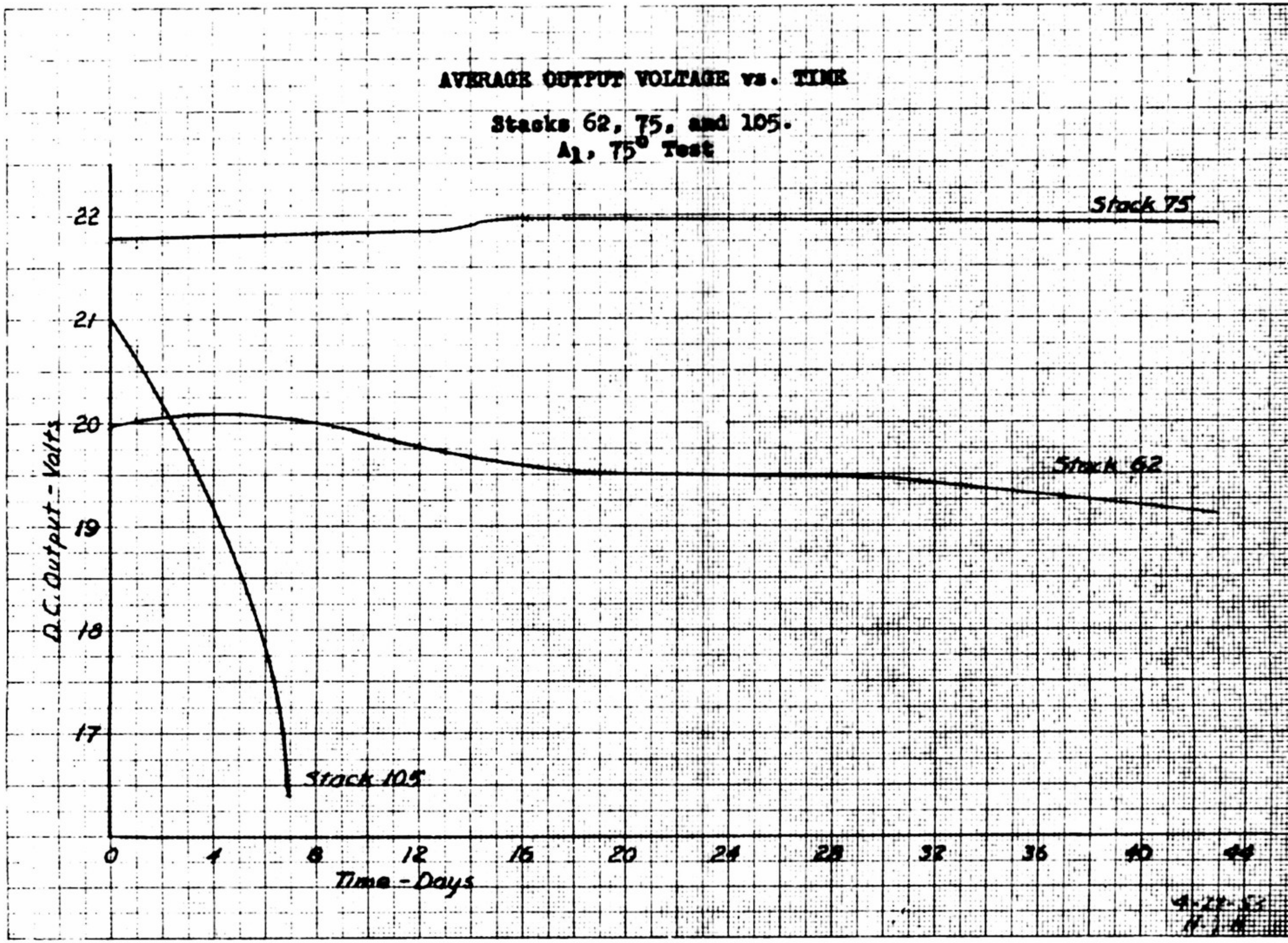
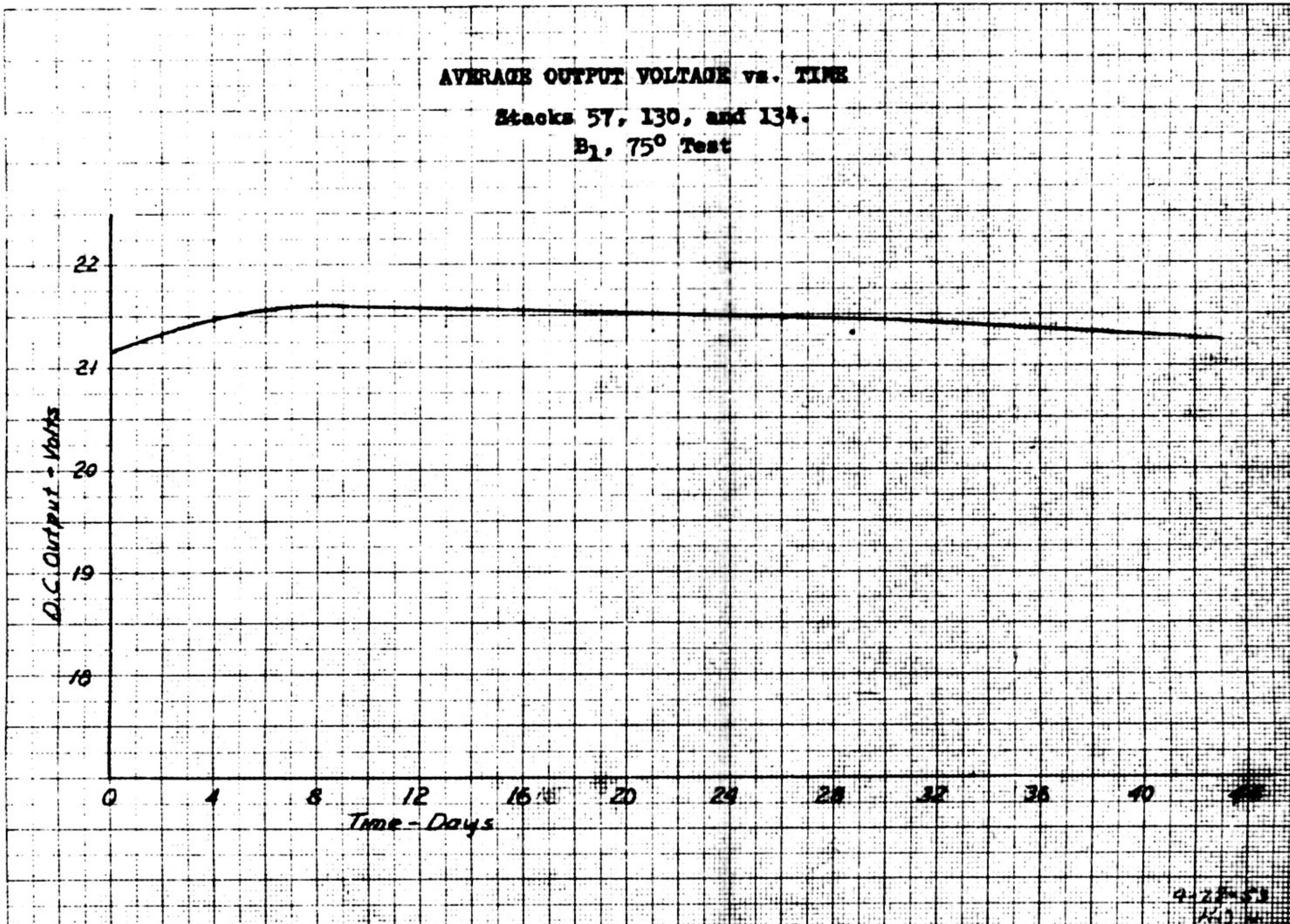

AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 86, 87, and 88.
C_2, 90° Test
Stacks 86 & 87
Stack 88
D.C. Output - Volts
22
21
20
19
0
4
8
12
16
20
24
28
Time - Days
11-15-52

Fig. 29



AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 62, 75, and 105.
A_1, 75° Test
Stack 75
Stack 62
Stack 105
22
21
20
19
18
17
D.C. Output - Volts
0
4
8
12
16
20
24
28
32
36
40
44
Time - Days

Fig. 30



AVERAGE OUTPUT VOLTAGE vs. TIME
Stacks 57, 130, and 134.
B_1, 75° Test
22
21
20
19
18
D.C. Output - Volts
0
4
8
12
16
20
24
28
32
36
40
Time - Days

Fig. 31

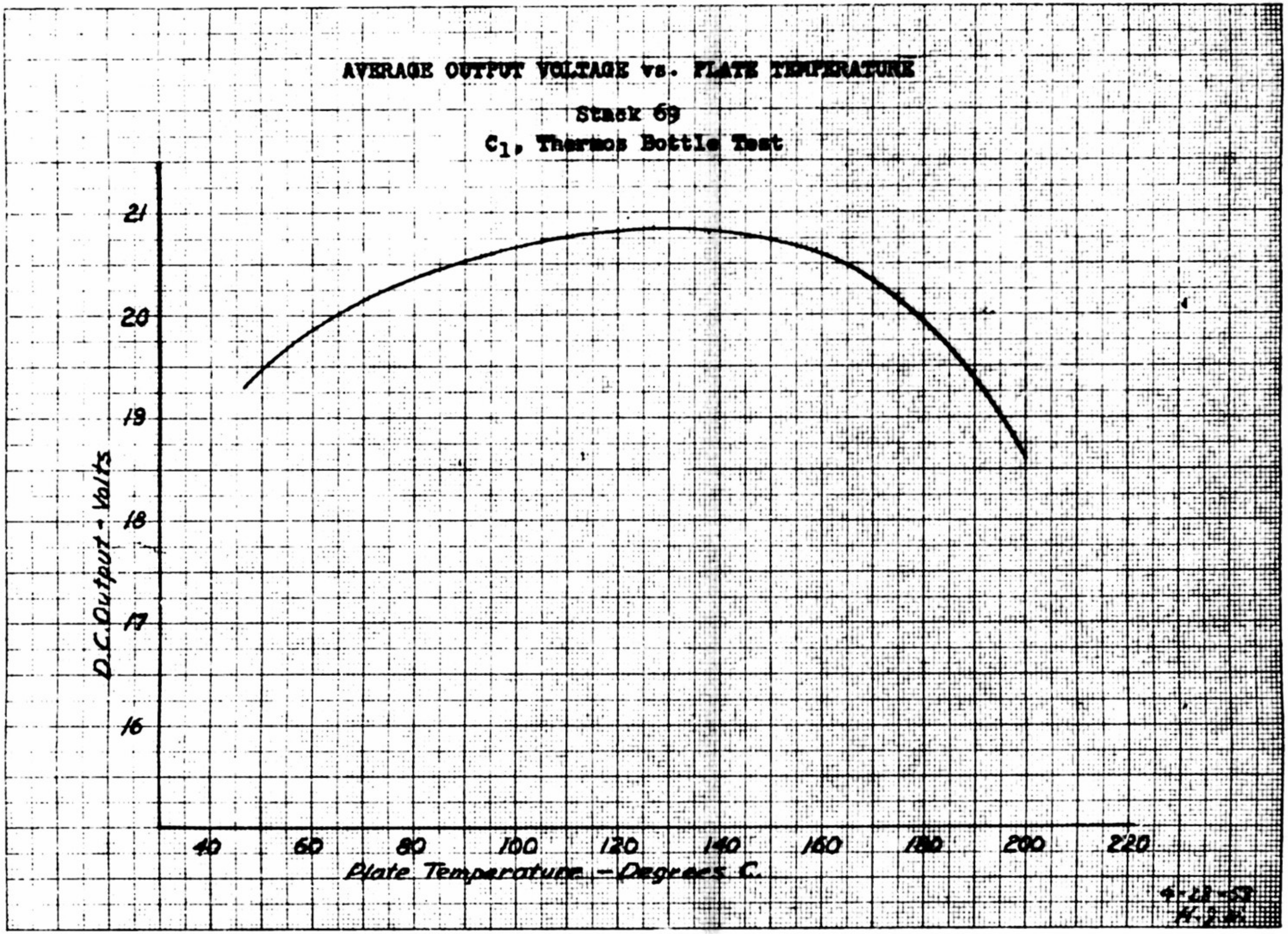

AVERAGE OUTPUT VOLTAGE vs. PLATE TEMPERATURE
Stack 69
C_1, Thermos Bottle Test
D.C. Output - Volts
21
20
19
18
17
16
40
60
80
100
120
140
160
180
200
220
Plate Temperature - Degrees C.

Fig. 32

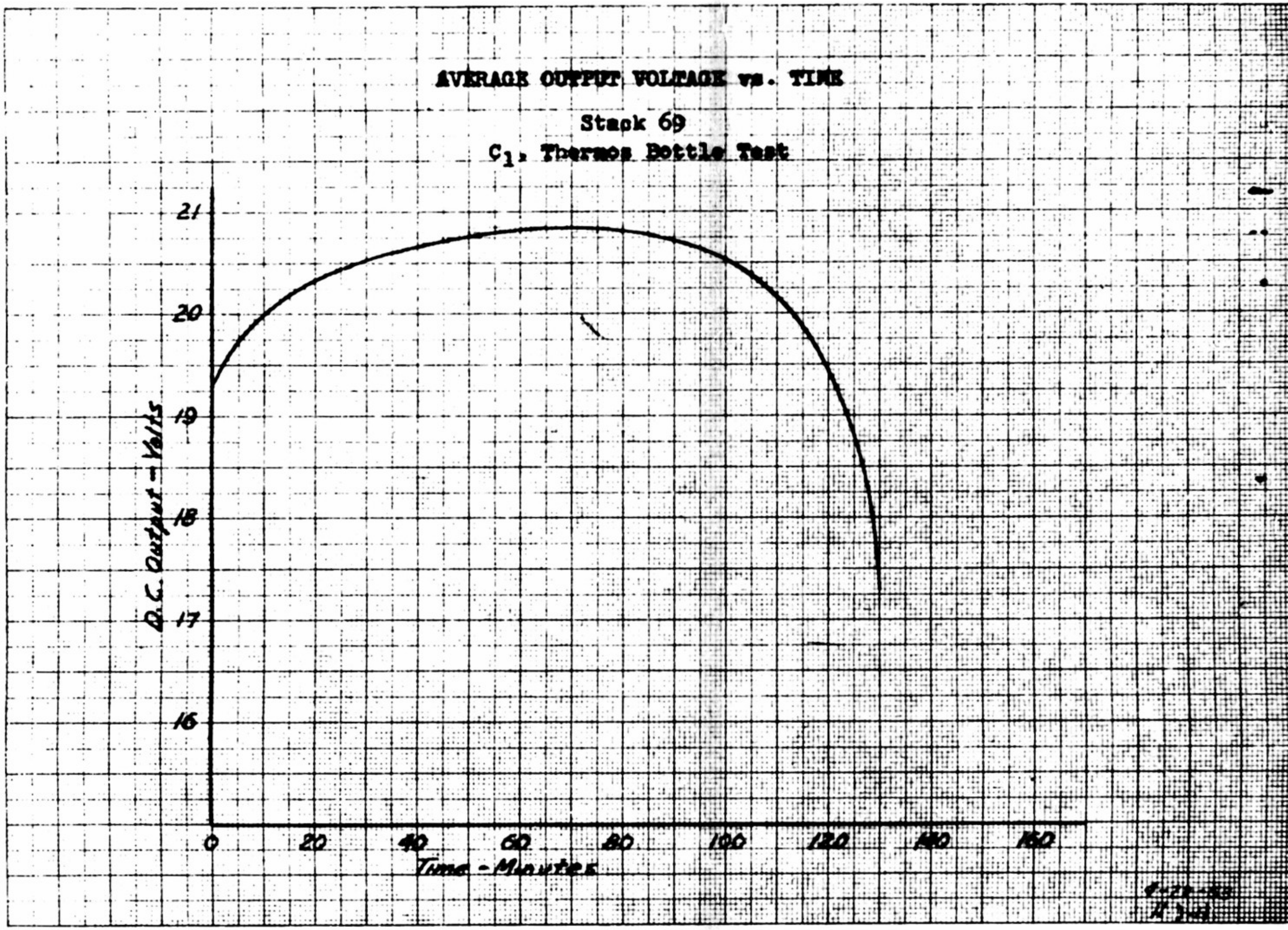
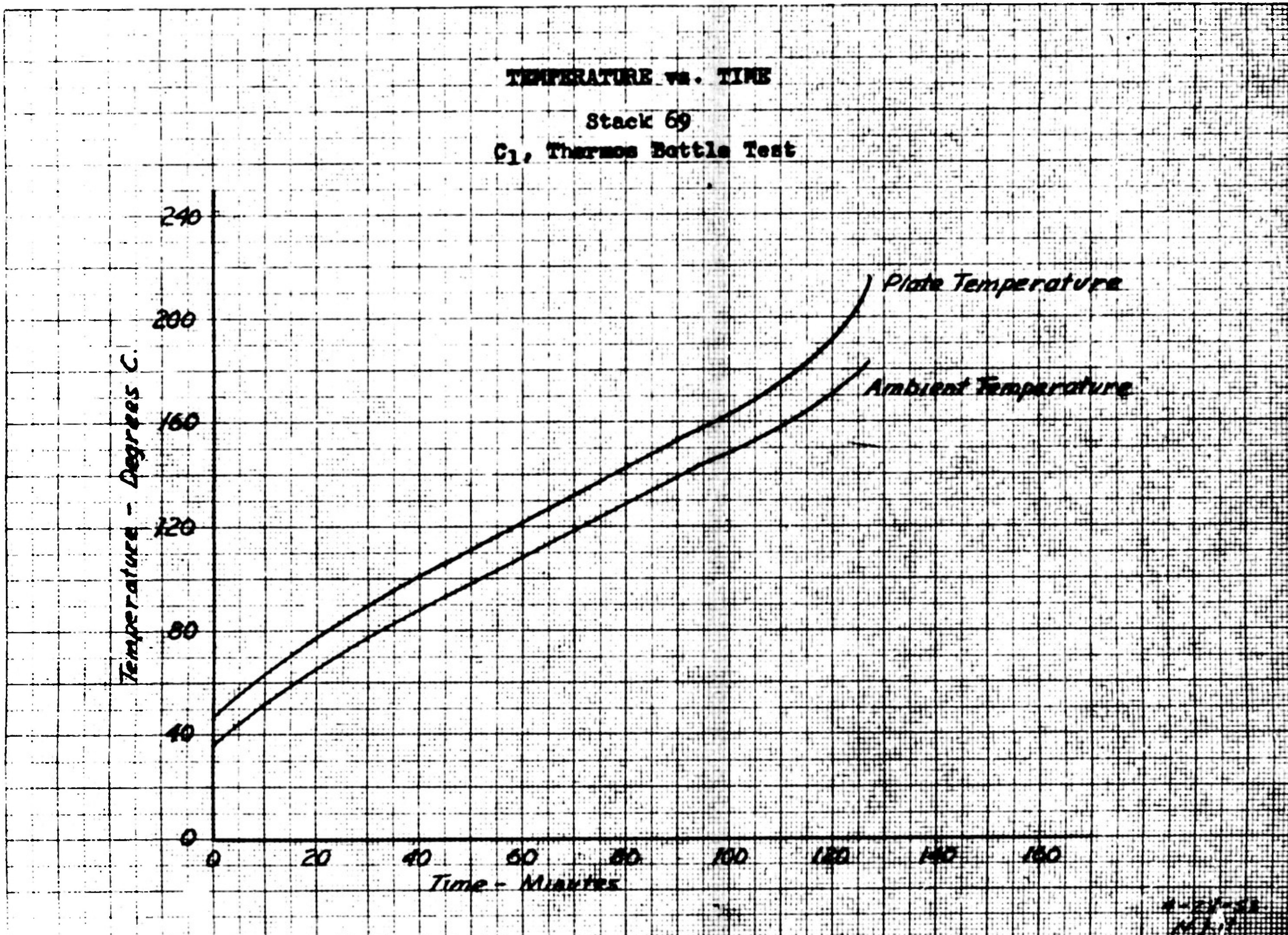

AVERAGE OUTPUT VOLTAGE vs. TIME
Stack 69
C1, Thermos Bottle Test
21
20
19
18
17
16
D.C. Output - Volts
0
20
40
60
80
100
120
140
160
Time - Minutes

Fig. 33



TEMPERATURE vs. TIME
Stack 69
C_1, Thermos Bottle Test
Plate Temperature
Ambient Temperature
Temperature - Degrees C.
0
40
80
120
160
200
240
0
20
40
60
80
100
120
140
160
Time - Minutes

Fig. 34